

Broadband Power Amplifier Limitations due to Package Parasitics

Dušan N. Grujić¹, Lazar Saranovac²

Abstract: Limitations of CMOS broadband power amplifiers due to package parasitics have been explored in this paper. The constraints of power amplifier matching network, realized as a third-order Chebyshev filter, have been derived, and a new power amplifier design flow has been proposed. As an example of a proposed design flow, an UWB power amplifier has been designed. Transistor level large signal simulation results are in excellent agreement with theoretical predictions.

Keywords: Broadband, CMOS, Package, Power amplifier.

1 Introduction

Broadband CMOS power amplifiers are used in multitude of applications such as ultra-wideband communications, short range high-resolution RADAR systems, software-defined and flexible radios, and many other safety, security, industrial and medical applications. The prerequisite for massive deployment is low cost, implying the use of standard CMOS process, minimum chip area and common packaging technology. However, the package parasitics, specifically the minimum value of bond-wire inductance, impose limitations on achievable bandwidth and output power. Therefore, it is important to know whether the power amplifier specifications are realizable with a given CMOS process and packaging technology.

The fundamental limitations of broadband power amplifier have been reviewed in Section 2. A power amplifier matching network design flow, based on technology and bond-wire quality factors, making it independent of technology and frequency band, is presented in Section 3. Design example of ultra-wideband power amplifier operating in 3-6 GHz band is presented in Section 4. Final remarks and conclusion have been given in Section 5.

¹Lime Microsystems d.o.o., Omladinskih brigada 86p, 11070 Belgrade, Serbia; E-mail: d.grujic@limemicro.com

²School of Electrical Engineering, University of Belgrade, Bulevar kralja Aleksandra 73, 11120 Belgrade, Serbia; E-mail: laza@etf.rs

2 Fundamental Limitations of Broadband Power Amplifier

Power amplifier’s output power is load dependant, and is maximized for a load impedance [1]:

$$Z_{opt} = R_{opt} \parallel \left[-\frac{1}{j\omega C_D} \right], \tag{1}$$

where R_{opt} is determined by biasing conditions:

$$R_{opt} = \frac{V_{max} - V_{min}}{2I_Q}, \tag{2}$$

and C_D is the capacitance seen at transistor drain. The term $(-j\omega C_D)^{-1}$ in (1) is inductive in nature, and cancels-out the transistor parasitic capacitance, while the R_{opt} term simply represents the optimum load-line resistance. Although inductive in nature, the imaginary part of optimum load impedance has an ω^{-1} frequency dependency, so it cannot be realized with an inductor – a more elaborate matching network is needed. It should also be noted that $(-j\omega C_D)^{-1}$ would result in cancellation of transistor parasitic capacitance at all frequencies, resulting in infinite bandwidth.

Optimum impedance for a unit transistor can be determined by Load-Pull simulation setup, shown in Fig. 1, where the unit transistor has NF fingers of width W_{finger} . The term “unit transistor” should be interpreted loosely, in the sense that transistor of any size can be considered as unit transistor. For an N times larger transistor, the optimum impedance is N times smaller.

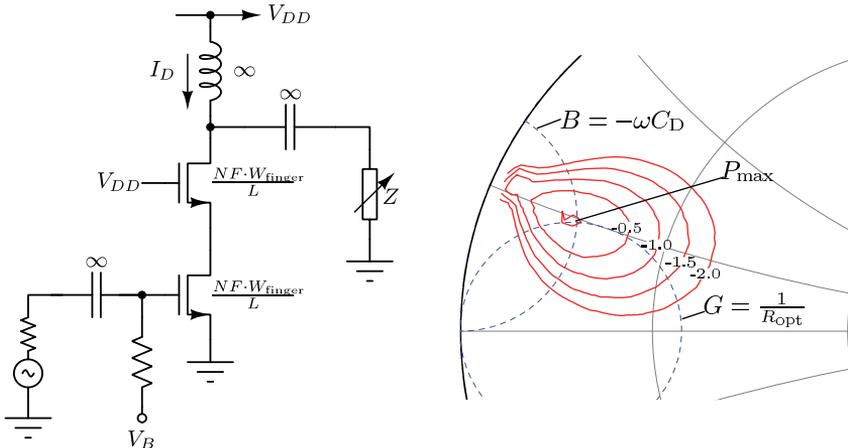


Fig. 1 – Cascode CMOS power amplifier Load-Pull setup.

Since the maximum output voltage is limited by transistor breakdown, optimum resistance can be scaled by increasing the bias current density per unit width and/or by increasing the transistor width W .

A comprehensive analysis of bias current density scaling and its effect on small- and large-signal parameters can be found in our previous work on the design of 60 GHz power amplifiers [2,3]. The designed 60 GHz power amplifiers have been fabricated in 0.25 μm SiGe:C HBT technology and measured on-wafer. Measurement results were in excellent agreement with theoretical predictions, validating the optimum impedance design approach given in (1), (2) and in Fig. 1.

Increasing the transistor width W reduces the optimum resistance $R_{\text{opt}} \sim W^{-1}$ and increases the parasitic capacitance $C_D \sim W$, but their product remains constant, and is a technology parameter [4]:

$$\tau = R_{\text{opt}} C_D = \text{const for technology} . \quad (3)$$

To achieve the maximum output power, the matching network should transform the load impedance Z_0 , usually 50 Ω , to optimum impedance given by (1). Therefore, the problem of achieving the maximum output power reduces to a problem of matching the source of resistance R_{opt} in parallel with capacitance C_D to a resistive load Z_0 .

Fundamental limitations of matching the complex to real impedance have been studied by Bode [5], Fano [6], Youla [7] and others, while the practical applications have been studied by Levy, Dawson and others [8,9]. The most important result is the Bode-Fano criterion, which formulates the fundamental limitation of matching a load resistance R with shunt capacitance C :

$$\int_0^\infty \ln \frac{1}{|\rho|} d\omega \leq \frac{\pi}{RC}, \quad (4)$$

where ρ is the reflection coefficient at the input of matching network. Criterion (4) states that the area under the curve $\ln|\rho|^{-1}$ is bounded, and is valid for arbitrary lossless and reciprocal matching network. Since the matching network is assumed to be lossless and reciprocal, the sum of reflected and transmitted power is equal to the source power. Therefore, for a specified in-band ripple the power amplifier bandwidth is limited by the RC product. Consequently, it is not possible to transform the real load to optimum load impedance (1), i.e. cancel the transistor parasitic capacitance, over an infinite bandwidth by an arbitrary lossless reciprocal network, even if the network order tends to infinity.

Bode-Fano criterion has an important implication regarding the shape of the power transfer function. Maximum bandwidth can be achieved by designing

a matching network with a brick-wall band-pass response, where the power is transmitted only in the frequency band of interest and reflected otherwise. This can be easily verified by inspection of (4), because the regions of total reflection, where reflection coefficient $|\rho|=1$, do not contribute to the area under the curve. Since the brick-wall frequency response is not realizable, the Chebyshev type I filter is commonly used, because it has the steepest roll-off in the class of all-pole filters.

3 Power Amplifier Output Matching Network Design

The design of band-pass all-pole Chebyshev matching network starts with the generic third order network shown in Fig. 2. For a specified frequency band (ω_L, ω_H) and in-band gain ripple ε , the third order band-pass Chebyshev filter element values are given by:

$$\omega_0 = \sqrt{\omega_H \omega_L}, \quad \Delta = \frac{\omega_H - \omega_L}{\omega_0}, \quad (5)$$

$$C_1 = \frac{g_1}{\omega_0 \Delta Z_0}, \quad L_1 = \frac{\Delta Z_0}{\omega_0 g_1}, \quad (6)$$

$$C_2 = \frac{\Delta}{\omega_0 g_2 Z_0}, \quad L_2 = \frac{g_2 Z_0}{\omega_0 \Delta}, \quad (7)$$

$$C_3 = \frac{g_3}{\omega_0 \Delta Z_0}, \quad L_3 = \frac{\Delta Z_0}{\omega_0 g_3}, \quad (8)$$

$$g_1 = \frac{1}{\gamma}, \quad g_2 = \frac{2\gamma}{\gamma^2 + \frac{3}{4}}, \quad g_3 = \frac{1}{\gamma}, \quad (9)$$

$$\gamma = \sinh\left(\frac{\beta}{6}\right), \quad (10)$$

$$\beta = \ln \coth\left(\frac{R_{\text{dB}}}{40 \log e}\right) = \ln \coth\left(\frac{\ln(1 + \varepsilon^2)}{4}\right) = 2 \sinh^{-1}\left(\frac{1}{\varepsilon}\right), \quad (11)$$

where ω_0 is the center frequency, Δ is the fractional bandwidth and R_{dB} is the in-band ripple expressed in decibels.

For small values of in-band ripple, β can be expanded to generalized Puiseux series, leading to approximation of γ :

$$\ln \coth(x) = -\ln(x) + \frac{x^2}{3} - \frac{7x^4}{90} + O(x^6) \approx -\ln(x)|_{x \ll 1}, \quad (12)$$

$$\gamma \approx \sinh \ln \sqrt[6]{\frac{40 \log e}{R_{dB}}} = \sinh \ln \sqrt[6]{\frac{4}{\ln(1 + \varepsilon^2)}}. \quad (13)$$

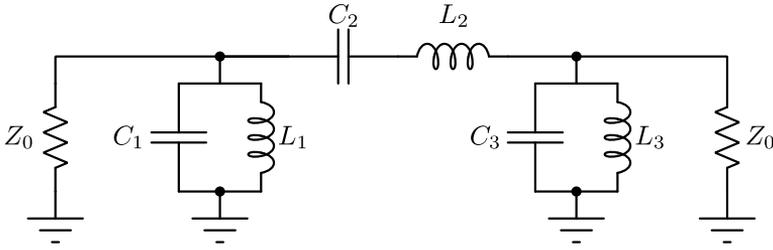


Fig. 2 – Generic all-pole third order LC band-pass filter.

Optimum resistance R_{opt} is usually smaller than 50Ω , so it is necessary to perform impedance transformation as well. Impedance transformation can be achieved by using the capacitive Norton transformation, shown in Fig. 3.

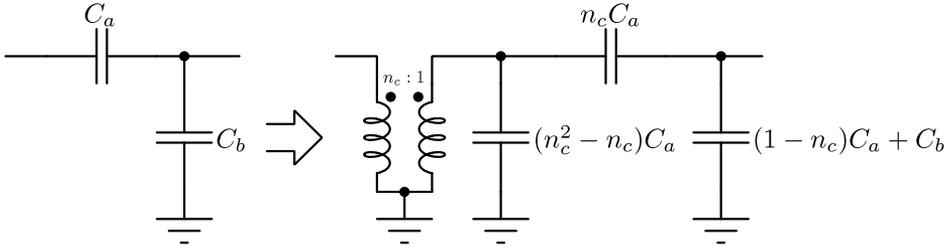


Fig. 3 – Capacitive Norton transformation.

Maximum impedance transformation ratio is limited by the constraint that all element values must be positive:

$$(1 - n_c)C_2 + C_3 \geq 0, \quad (14)$$

$$n_c \leq n_{cmax} = 1 + \frac{g_2 g_3}{\Delta^2} = 1 + \frac{g_1 g_2}{\Delta^2}. \quad (15)$$

Larger impedance transformation ratio can be achieved only by adding a physical on- or off-chip transformer.

Applying the capacitive Norton transformation to elements C_2 and C_3 in the filter from Fig. 2, we get the transformed band-pass filter shown in Fig. 4. It has a structure of packaged power amplifier with two external elements. Our

goal is to design a filter so that the elements marked as “Transistor” in Fig. 4 are equal to optimum resistance and parasitic capacitance:

$$R_{\text{opt}} = \frac{Z_0}{n_c^2} \text{ and } C_D = n_c^2 C_1. \quad (16)$$

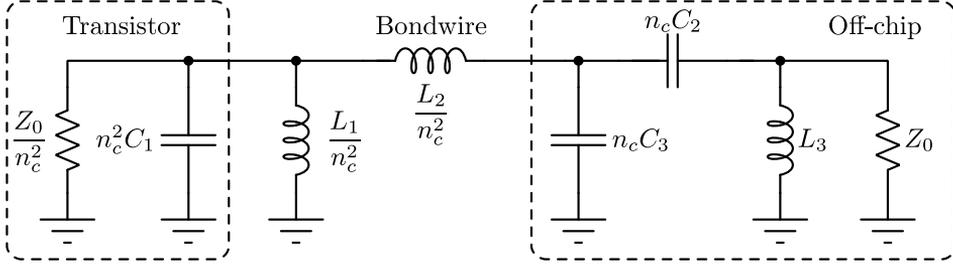


Fig. 4 – Transformed band-pass filter.

For a given center frequency ω_0 we can define the technology quality factor Q_T and bond-wire quality factor Q_L as:

$$Q_T = R_{\text{opt}} C_D \omega_0 = \tau \omega_0, \quad (17)$$

$$Q_L = \frac{L_{\text{bond}} \omega_0}{Z_0}. \quad (18)$$

Both quality factors are independent of output power and fractional bandwidth.

Combining (16), (9) and (6) we get:

$$R_{\text{opt}} C_D = \frac{Z_0}{n_c^2} n_c^2 C_1 = \frac{g_1}{\omega_0 \Delta}, \quad (19)$$

$$g_1 = Q_T \Delta, \quad (20)$$

$$Q_T \Delta \gamma = 1. \quad (21)$$

Expression (21) is very important, since it reveals that for a fixed technology quality factor Q_T wider bandwidth must be traded for more in-band ripple. This conclusion is consistent with Bode-Fano criterion (4).

The Norton transformation ratio can be expressed in terms of technology quality factor Q_T and fractional bandwidth Δ as:

$$n_c = 1 + \frac{8Q_T^2}{4 + 3Q_T^2 \Delta^2}. \quad (22)$$

From (22) it can be seen that wider bandwidth results in lower impedance transformation ratio, and hence lower output power.

More insight into relations between technology and bond-wire quality factors and fractional bandwidth can be obtained by expressing the bond-wire inductance in terms of filter design parameters:

$$L_{\text{bond}} = \frac{L_2}{n_c^2} = \frac{\frac{g_2 Z_0}{\omega_0 \Delta}}{\left(1 + \frac{g_1 g_2}{\Delta^2}\right)^2}. \quad (23)$$

Substituting (7), (9), (18) and (21) into (23) we get:

$$Q_L = \frac{8Q_T(3Q_T^2\Delta^2 + 4)}{\left[Q_T^2(3\Delta^2 + 8) + 4\right]^2}. \quad (24)$$

Setting $\delta = \Delta^2$ and solving (24) for δ results in:

$$\delta_{1,2} = \frac{4Q_T(1 \pm \sqrt{1 - 4Q_T Q_L}) - Q_L(1 + 2Q_T^2)}{3Q_T^2 Q_L}. \quad (25)$$

The fractional bandwidth Δ must be real, and so must $\delta = \Delta^2$, resulting in the restriction of technology and bond-wire quality factors:

$$Q_T Q_L \leq \frac{1}{4}. \quad (26)$$

Furthermore, δ must be non-negative for fractional bandwidth to be real. Solving (25) for $\delta = 0$ results in:

$$\delta_{1,2} = 0 \Rightarrow Q_L = \frac{2Q_T}{(2Q_T^2 + 1)^2}. \quad (27)$$

Only one solution of (25) can be zero for a given Q_T :

$$\delta_{1,2} = 0 \begin{cases} \delta_1, Q_T \in \left(0, \frac{\sqrt{2}}{2}\right) \\ \delta_2 \text{ otherwise} \end{cases} \quad (28)$$

Taking partial derivatives of (25) can reveal more restrictions and regions of interest in the $Q_T - Q_L$ plane:

$$\frac{\partial \delta_{1,2}}{\partial Q_T} = \frac{4(2Q_L - Q_T)\sqrt{1 - 4Q_T Q_L} \pm Q_T(2Q_L Q_T - 1)}{3Q_T^3 Q_L \sqrt{1 - 4Q_T Q_L}} \quad (29)$$

Maximum value of δ_1 for a given Q_T is on the curve where partial derivative with respect to Q_L is zero:

$$\frac{\partial \delta_1}{\partial Q_L} = 0 \Rightarrow Q_L = \frac{1 + Q_T^2(4 - Q_T^2) \pm (Q_T^2 - 1)\sqrt{Q_T^2(Q_T^2 - 6) + 1}}{8Q_T}. \quad (30)$$

Solving (27) and (30) results in values of Q_T and Q_L for which maximum value of δ_1 is zero:

$$\delta_1 = 0 \wedge \frac{\partial \delta_1}{\partial Q_T} = 0 \Rightarrow Q_T = \frac{\sqrt{6}}{6}, Q_L = \frac{3\sqrt{6}}{16}. \quad (31)$$

This point is important, since it gives the largest value of Q_L , or equivalently absolute maximum of bond-wire inductance, which can be absorbed by the filter. For example, for a center frequency of 1 GHz the maximum value of bond-wire inductance is approximately 3.7 nH and scales inversely proportional to frequency. This simple rule-of-the-thumb can be used to quickly estimate whether the design is feasible or not.

Examining the remaining three partial derivatives in regions where $\delta_{1,2}$ are non-negative and real results in:

$$\delta_1 \geq 0 \wedge \delta_1 \in \mathbb{R} \Rightarrow \frac{\partial \delta_1}{\partial Q_L} < 0, \quad (32)$$

$$\delta_2 \geq 0 \wedge \delta_2 \in \mathbb{R} \Rightarrow \frac{\partial \delta_2}{\partial Q_T} > 0, \quad (33)$$

$$\delta_2 \geq 0 \wedge \delta_2 \in \mathbb{R} \Rightarrow \frac{\partial \delta_2}{\partial Q_L} > 0. \quad (34)$$

Results (25)–(34) provide enough information to draw Fig. 5, which shows the regions where non-negative and real solutions $\delta_{1,2}$ exist in the $Q_T - Q_L$ plane. Non-negative and real solution δ_1 exists for all values of $Q_T > 0$, and is bounded by $\delta_1 = 0$ (27) for $Q_T \leq \sqrt{2}/2$ (positive-negative boundary), and $4Q_T Q_L \leq 1$ otherwise (complex-real boundary). Non-negative and real solution δ_2 exists for $Q_T \geq \sqrt{2}/2$, and is bounded by $\delta_2 = 0$ (27) and $4Q_T Q_L \leq 1$.

From a practical point of view, boundary contours in Fig. 5 show that there is a maximum value of bond-wire inductance which can be absorbed into the filter with maximum Norton transformation ratio. Since the length, or

equivalently inductance and Q_L , of bond-wire is limited by the used package, it cannot be arbitrary small. Consequently there is a maximum value of Q_T , which corresponds to minimum practical value of Q_L . As we will show, maximum value of Q_T , due to physical constraints of bond-wire length, limits the achievable maximum output power.

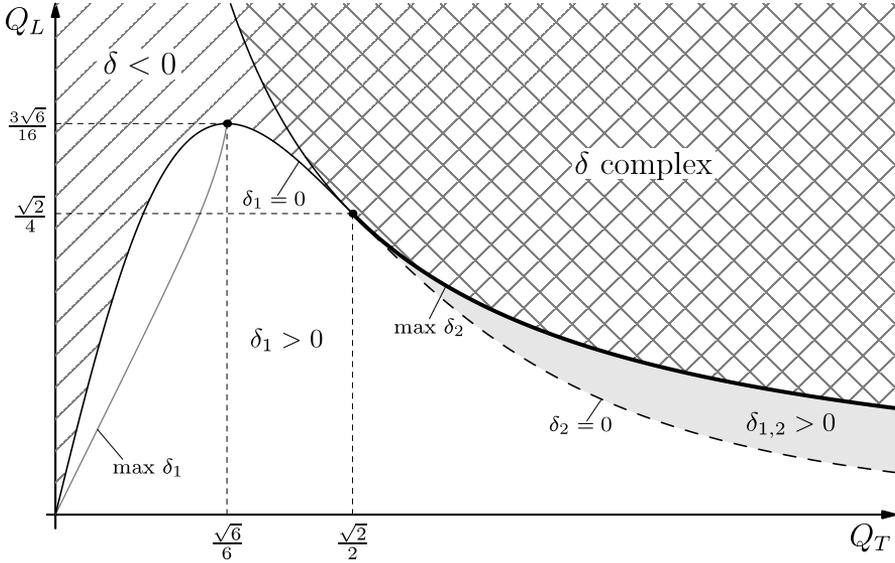


Fig. 5 – Squared fractional bandwidth δ boundary contours in the $Q_T - Q_L$ plane.

The Norton transformation ratio can be expressed in terms of technology quality factor Q_T and bond-wire quality factor Q_L by substituting $\delta_{1,2}$ solutions (25) into (22), resulting in:

$$n_{c1,2} = \frac{1 \mp \sqrt{1 - 4Q_T Q_L}}{2Q_T Q_L}. \quad (35)$$

Condition for maximum Norton transformation ratio coincides with $\delta = 0$ (27). Maximum Norton transformation ratio is then:

$$n_{cmax} = 1 + 2Q_T^2. \quad (36)$$

This result can be easily verified by substituting $\Delta^2 = 0$ into (22). Therefore, a maximum value of technology quality factor Q_T , due to physical constraints of bond-wire length, limits the maximum impedance transformation ratio and hence the output power.

Condition that maximum output power is achieved for zero fractional bandwidth might seem paradoxical, since the amplifier with zero bandwidth is of no use. However, the resolution to this apparent paradox is in the definition of Chebyshev filter fractional bandwidth, which is referred to in-band ripple:

$$|H(j)|^2 = \frac{1}{1 + \varepsilon^2 T_n^2(1)} = \frac{1}{\varepsilon^2}, \quad (37)$$

where T_n is the Chebyshev polynomial of n th order. This can be seen from (21), which is rewritten again for clarity:

$$Q_T \Delta \gamma = 1.$$

If we let fractional bandwidth $\Delta \rightarrow 0_+$ then $\gamma \rightarrow \infty$, resulting in infinitely small in-band ripple, but their product is finite and equal to Q_T^{-1} .

Bandwidth for a conventional definition of A dB loss is wider by a factor Ω which can be calculated from (37):

$$10 \log(1 + \varepsilon^2 T_n^2(\Omega)) = A. \quad (38)$$

Solving (38) for Ω results in:

$$\Omega_n(A, \varepsilon) = \cosh\left(\frac{1}{n} \cosh^{-1} \frac{\varepsilon_A}{\varepsilon}\right), \quad (39)$$

where

$$\varepsilon_A = \sqrt{10^{\frac{A}{10}} - 1}. \quad (40)$$

Effective fractional bandwidth, defined for A dB loss is then:

$$\Delta_{A,\varepsilon} = \Delta \Omega_n(A, \varepsilon). \quad (41)$$

Substituting (10), (11) and (21) into (41) results in the expression:

$$\Delta_{A,\varepsilon} = \frac{1}{Q_T} \frac{\cosh\left(\frac{1}{n} \cosh^{-1} \frac{\varepsilon_A}{\varepsilon}\right)}{\sinh\left(\frac{1}{n} \sinh^{-1} \frac{1}{\varepsilon}\right)} = \frac{1}{Q_T} \Theta_n(A, \varepsilon), \quad (42)$$

where $\Theta_n(A, \varepsilon)$ is the quality factor-independent part of effective fractional bandwidth.

Although the Chebyshev filter fractional bandwidth tends to zero as in-band ripple tends to be infinitesimally small:

$$\lim_{\varepsilon \rightarrow 0_+} \Delta = 0, \quad (43)$$

effective A dB fractional bandwidth is finite for finite Q_T :

$$\Delta_{A,0_+} = \frac{1}{Q_T} \lim_{\varepsilon \rightarrow 0_+} \Theta_n(A, \varepsilon) > 0. \quad (44)$$

To the best of authors knowledge, function $\Theta_n(A, \varepsilon)$ cannot be simplified, even when $\varepsilon \rightarrow 0_+$, but can be evaluated numerically. Several numerical values for third order filter $\Theta_3(A, 0_+)$ versus bandwidth definitions are given in **Table 1**.

Table 1
Values of function $\Theta_3(A, 0_+)$ for several bandwidth definitions.

A [dB]	0.01	0.10	0.20	0.50	1.00	3.00
$\Theta_3(A, 0_+)$	0.363	0.534	0.601	0.704	0.798	0.999

Finite bandwidth for zero Chebyshev filter fractional bandwidth means that the maximum transformation ratio, given in (36), can be used in power amplifier design. A closer examination of **Table 1** and (44) reveals that effective fractional bandwidth can be even larger than one for small values of technology quality factor Q_T , enabling the design of broadband amplifiers.

Presented results can be used in the design of broadband power amplifiers in a CAD environment. Contours of constant transformation ratio and effective fractional bandwidth can be very helpful, and provide a quick insight into possible trade-offs.

Constant transformation ratio n_c contour can be derived from (35) by solving for Q_L :

$$Q_L = \frac{n_c - 1}{n_c^2 Q_T} \Big|_{Q_T > \sqrt{\frac{n_c - 1}{2}}}. \quad (45)$$

The restriction for technology quality factor Q_T comes from requirements that the fractional bandwidth is non-negative and real. Having in mind that maximum Q_L is decreasing with Q_T , maximum transformation ratio might be limited by the minimum bond-wire length for a given package.

Contours of constant effective fractional bandwidth can be derived by substituting (10), (11) and (21) into (42) and expressing the effective fractional bandwidth in terms of γ :

$$\Delta_A = \frac{\cosh\left(\frac{1}{3} \cosh^{-1}\left(\gamma A(4\gamma^2 + 3)\right)\right)}{\gamma Q_T}, \quad (46)$$

where

$$\gamma_{1,2} = \frac{1}{Q_T \sqrt{\delta_{1,2}}}, \quad (47)$$

and $\delta_{1,2}$ are given in (25). Constant effective fractional bandwidth contours do not have a closed form solution, but can be drawn by a computer program.

4 Ultra-Wideband Power Amplifier Design Example

The application of the results derived in the previous section will be demonstrated on the design of packaged cascode CMOS UWB power amplifier for 3-6 GHz band in 180 nm technology. The desired output 1 dB compression point is set at 15 dBm, with a flatness of 0.1 dB in the whole operating band. The operating band sets the requirement for center frequency of:

$$f_0 = \sqrt{f_H f_L} \approx 4.24 \text{ [GHz]}, \quad (48)$$

and effective 0.1 dB fractional bandwidth of:

$$\Delta_{0.1 \text{ dB}} = \frac{f_H - f_L}{f_0} = \frac{\sqrt{2}}{2} \approx 0.71. \quad (49)$$

As a first step, technology time constant τ has to be determined. Optimum load resistance and parasitic capacitance have been determined from a large signal Load-Pull simulation by using the setup shown in Fig. 1. The unit transistor was chosen to have a minimum gate length and width of:

$$W_{\text{unit}} = NF \cdot W_{\text{finger}} = 8 \cdot 5 = 40 \text{ [\mu m]}. \quad (50)$$

The transistor was biased with a drain current of $I_{D,\text{unit}} = 4 \text{ [mA]}$. Optimum load resistance and parasitic capacitance of unit transistor were determined to be:

$$R_{\text{opt,unit}} = 360 \text{ }\Omega \text{ and } C_{D,\text{unit}} = 48 \text{ [fF]}. \quad (51)$$

Technology time constant is:

$$\tau = R_{\text{opt}} C_D = 17.28 \text{ [ps]}, \quad (52)$$

and technology quality factor at band center frequency is:

$$Q_T = \tau \omega_0 \approx 0.46. \quad (53)$$

Unit transistor output power at 1 dB compression, when loaded with optimum impedance (1), is also determined from Load-Pull simulation:

$$P_{1 \text{ dB,unit}} = 2.5 \text{ [dBm]} \quad (1.8 \text{ [mW]}). \quad (54)$$

To achieve the desired output 1 [dB] compression power, the power amplifier transistor should be N times larger than the unit transistor, where the ratio is:

$$N = \frac{P_{1 \text{ dB}}}{P_{1 \text{ dB,unit}}} = 18. \quad (55)$$

The optimum resistance of N times larger transistor is

$$R_{\text{opt}} = \frac{R_{\text{opt,unit}}}{N} = 20 \text{ } [\Omega], \quad (56)$$

from which the required impedance transformation ratio can be calculated:

$$n_c^2 = \frac{Z_0}{R_{\text{opt}}} = \frac{50}{20} = 2.5. \quad (57)$$

The calculated parameters have been used to draw constant effective fractional bandwidth and transformation ratio contours shown in Fig. 6. The cross-hatched area represents unrealizable solutions, since they require technology quality factor smaller than the quality factor of used technology. Larger technology quality factor can be achieved by adding shunt capacitance at transistor drain node. The red and blue curves bound the area where the fractional bandwidth is larger than minimally required. The red curve is drawn for solution δ_1 while the blue curve is drawn for solution δ_2 . Constant transformation ratio curve, shown in black dashed line, is the locus of points having the specified output 1 dB compression power.

There are three solutions having the specified output power and exactly the specified bandwidth, and infinitely many solutions having the specified power and wider bandwidth. Wider bandwidth can be beneficial, since it provides some margin in case of process variations. From a theoretical point of view, all of possible solutions satisfy the requirements, and are therefore acceptable. However, from a practical point of view, the solution with maximum value of Q_L is desirable, because it results in maximum bond-wire inductance, or equivalently maximum bond-wire length. The chosen solution (0.539,0.431), marked with a dot, has maximum Q_L and results in effective 0.1 dB fractional bandwidth of approximately one. It is interesting to note that for this particular solution, the Chebyshev filter fractional bandwidth is $\Delta = 0$, allowing us to demonstrate the concepts shown in (37) – (44).

Matching network elements can now be determined for $\hat{Q}_T = 0.539$ by calculating limits of (6) – (8) for $\Delta \rightarrow 0_+$:

$$C_1 = \frac{\hat{Q}_T}{\omega_0 R_{\text{opt}}} \approx 1 \text{ [pF]}, \quad (58)$$

$$L_1 = \lim_{\Delta \rightarrow 0_+} \frac{\Delta Z_0}{\omega_0 g_1 n_c^2} = \frac{Z_0}{\hat{Q}_T \omega_0 n_c^2} \approx 1.4 \text{ [nH]} \quad (59)$$

$$L_2 = L_{\text{bond}} = \lim_{\Delta \rightarrow 0_+} \frac{g_2 Z_0}{\omega_0 \Delta n_c^2} = \frac{2\hat{Q}_T Z_0}{\omega_0 n_c^2} \approx 810 \text{ [pH]}, \quad (60)$$

$$C_2 = \lim_{\Delta \rightarrow 0_+} \frac{n_c g_3}{\omega_0 \Delta Z_0} = \frac{n_c \hat{Q}_T}{\omega_0 Z_0} \approx 640 \text{ [fF]}, \quad (61)$$

$$C_3 = \lim_{\Delta \rightarrow 0_+} \frac{n_c \Delta}{\omega_0 g_2 Z_0} = \frac{n_c}{2\hat{Q}_T \omega_0 Z_0} \approx 1.1 \text{ [pF]}, \quad (62)$$

$$L_3 = \lim_{\Delta \rightarrow 0_+} \frac{\Delta Z_0}{\omega_0 g_3} = \frac{Z_0}{\hat{Q}_T \omega_0} \approx 3.5 \text{ [nH]}. \quad (63)$$

Since the technology quality factor Q_T is smaller than the chosen quality factor \hat{Q}_T , additional capacitance should be added to transistor drain:

$$C_{\text{1ext}} = C_1 - NC_D \approx 136 \text{ [fF]}. \quad (1)$$

The designed power amplifier schematic is shown in Fig. 7.

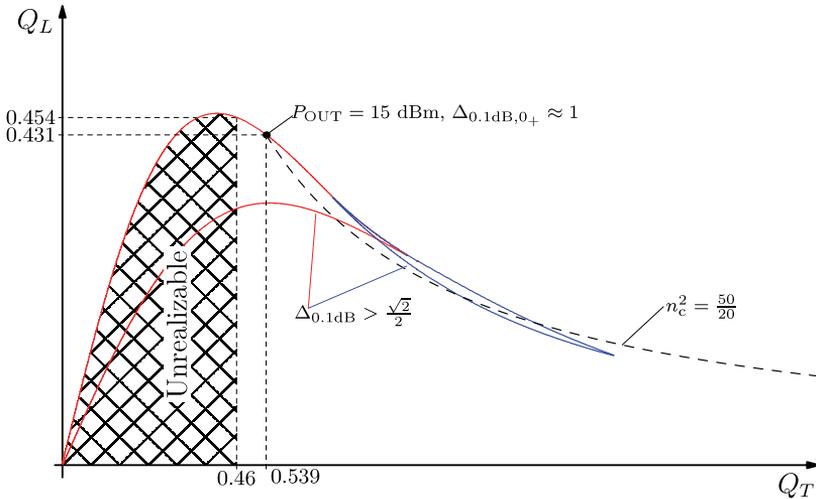


Fig. 6 – Constant 0.1 dB fractional bandwidth $\Delta_{0.1 \text{ dB}} = 0.71$ and constant transformation ratio $n_c^2 = 2.5$ contours in $Q_T - Q_L$ plane.

The power amplifier has only one integrated inductor, and absorbs the bond-wire inductance in a matching network. So instead of trying to compensate the bond-wire inductance, it is utilized to reduce the number of on-chip inductors. Per-unit length inductance for a typical bonding profile is around 1 nH/mm, so a bond-wire inductance of 0.81 nH corresponds to a bond-wire length of 0.8 mm. This bond-wire length is compatible with RF packages, so the designed power amplifier is realizable. The off-chip inductor can be a discrete inductor or a printed PCB inductor.

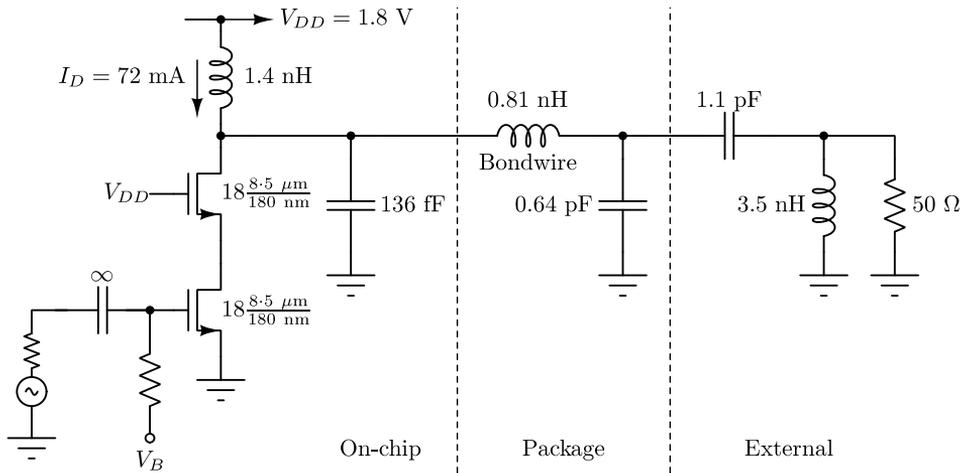


Fig. 7 – Designed power amplifier schematic.

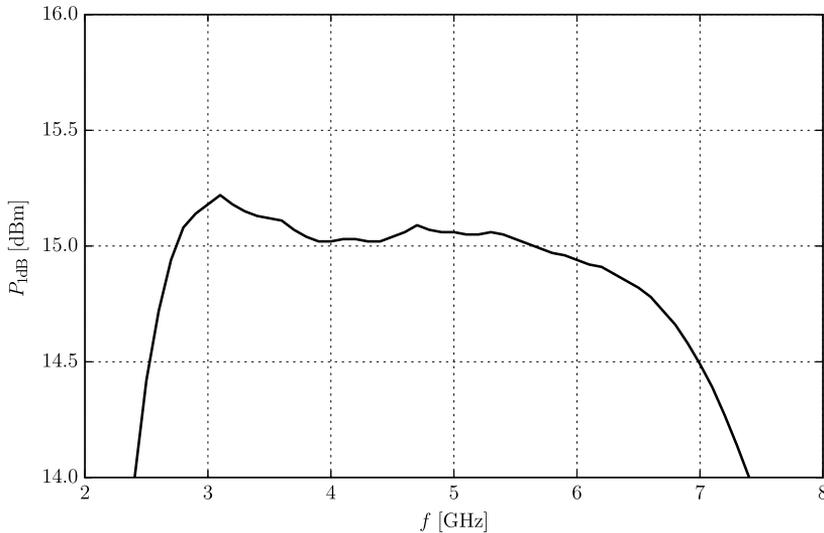


Fig. 8 – Simulated output power 1 dB compression point.

Designed power amplifier output power 1 dB compression point $P_{1\text{dB}}$ was simulated in Cadence Spectre circuit simulator in a frequency band of 2 to 8 GHz. The simulation results are shown in Fig. 8. It can be seen that the output power 1 dB compression point $P_{1\text{dB}}$ is almost constant in the specified frequency band of 3 to 6 GHz, and is within the designed 0.1 dB flatness, except at the lower band edge of 3 GHz. At lower band edge, the $P_{1\text{dB}}$ variation rises to 0.2 dB. Having in mind that the design flow is developed for an approximate model, and that simulation results are at transistor level, theoretical predictions and simulation results are in excellent agreement.

5 Conclusion

The limitations of broadband power amplifier due to bond-wire inductance have been examined in detail, and a new design flow has been proposed. By introducing the technology and bond-wire quality factors as design variables, the derived results are universal, and applicable to any technology and frequency band. Restrictions and regions of interest have been identified in the $Q_T - Q_L$ design space. It has been shown that the minimum bond-wire inductance limits the maximum transformation ratio, and consequently output power, for a third order band-pass Chebyshev matching network. Further improvements are only possible by using a matching network of higher order or a transformer. As a demonstration, a 3-6 GHz ultra-wideband CMOS power amplifier has been designed by using the proposed flow. Transistor-level large signal simulations are in excellent agreement with theoretical predictions.

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