A High Efficiency Non-Inverting Multi Device Buck-Boost DC-DC Converter with Reduced Ripple Current and Wide Bandwidth for Fuel Cell Low Voltage Applications

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Abstract: The voltage produced by the fuel cell (FC) device is unregulated and varies from 0.4 V to 0.8 V on full load to no-load respectively. When these devices are used in low voltage applications and output voltage lies between higher and lower values of input voltage range, it is required to connect a DC-DC buck-boost converter to get a fixed output voltage. In this paper, a new non-inverting multi device buck boost converter (MDBBC) is proposed, in which the multi device buck and boost converters are connected in cascade and operate individually either in buck or boost operating modes. The paper also includes the steady state analysis of MDBBC based on the state space averaging technique. A prototype model of proposed converter compatible with FCS-1000 Horizon FC model with rating of 270 W, 36 V is designed and developed. The proposed converter is experimentally validated with the results obtained from the prototype model, and results show the superiority of the converter with higher efficiency and lesser ripple current observed under steady state operation of the converter.

Keywords: Buck-Boost Converter, Multi Device Operation, Ripple Current Reduction, Buck-Boost Converters for Portable Applications.

1 Introduction

Fuel cell (FC) is a device which produces electrical energy by using the chemical energy of a fuel. The individual voltage of a single cell ranges from 0.4 V to 0.8 V from full load to no load respectively which gives a voltage regulation of approximately 100% [1]. As an individual cell voltage is very less, several FCs may be connected in series to form a stack and can realize the voltage requirement of the practical systems. For example, the Horizon FC model “FCS-1000” with 48 cells gives a rated voltage of 28 V at loaded condition and 45 V at no load. In many low power/voltage applications like battery charging/discharging, power factor correction and for extracting

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maximum power from solar photovoltaic (PV) panels, buck-boost converters may be used in obtaining a regulated voltage. As the fuel cell voltage is unregulated, step up/step down converter is compulsory to obtain a regulated output voltage which lies within the terminal voltage range of the FC stack [2 – 14]. The commonly used simple step up/step down converters buck-boost, Sepic, Cuk, and fly back topologies when used in the aforementioned applications, exhibits low efficiency, high device stress, and requires large value of filter inductor and capacitors and higher conduction losses [2].

In order to avoid high device stresses, paralleling or interleaved coupled inductors [3] and multilevel techniques are suggested in [4, 5]. But neither of the above approaches reduced voltage stress and current stress simultaneously. In order to achieve low device stress, high efficiency, lesser size of filter components, a cascaded buck-boost converter with independent controlled switches is suggested in [6], in which the converter operates only either in boost mode or buck mode depends on the input-output conditions. In [7 – 11] a non-inverting buck–boost converter (combining the boost and buck together results in single inductor) with high performance suitable for low voltage applications is suggested. But for higher voltages the usage of single inductor non–inverting buck boost converters results in high I/O pulsating currents, high noise levels, difficulty to control and limit the currents, to eliminate these problems a double inductor (one at the input and other at output) cascaded buck-boost converter has been proposed by [12 – 14].

A single phase cascaded buck-boost converter (BBC) with magnetic coupling between input inductor and output filter inductor has been proposed in [15], which reports higher efficiency, wide bandwidth, reduced input and output capacitor sizes, but the ripple current remains high. To overcome which a tri-state two switch buck-boost converter is have been proposed in [16], but the larger boost inductor is preferred which increases the size. Furthermore, some researchers have suggested pseudo CCM method to reduce the FC ripple current further [17, 18]. A two phase interleaved buck-boost converter (IBBC) with fewer ripples in the input current has been proposed in [19, 20]. Apart from the above mentioned BBC and IBBC another possible method is multi device technique, in which the component size of inductive and capacitive filters on input and output are reduced by simply increasing the frequency of ripple current in the inductor using parallel switches in a phase [21], however the switching and conduction losses, device stress, and number of current sensors are same as that of device switch buck-boost converters.

This paper presents a new multi device buck–boost converter (MDBBC) for FC low power applications. In MDBBC two switches are connected in parallel on buck and boost side as illustrated in Fig. 1a, resulting in a single inductor, doubling in effective switching frequency of the inductor ripple
current and thereby reducing the sizes of I/O filter components with higher bandwidth and same fault tolerance capability as IBBC. Further, the steady state operation of the proposed converter and state equations are derived on considering certain operating conditions and thereby the circuit design and implementation suitable for FC voltage regulation is presented. A prototype model of proposed converter is developed with 270 W, 36 V rating, which suits for FC voltage regulation purpose.

2 Proposed MDBBC Structure

The structure of MDBBC is depicted in Fig. 1a and consists of two switches and diodes connected in parallel per phase. By using multi devices per phase the sizes of the filter components are reduced by increasing the effective inductor ripple frequency and voltage ripple frequency. A phase shifting mechanism is used to provide the doubled ripple frequency (100 kHz) in the buck and boost inductors ripple current at the same device switching frequency (50 kHz), which can provide a larger system bandwidth. The larger bandwidth helps in achieving the high speed dynamic response for the converter and also reduces the sizes of the filtering components.

![Proposed converter and operating modes: a) schematic circuit of the proposed converter; b) Activation signals for the buck and boost switches; c) operating modes of the converter in both buck and boost operations.](image)

Fig. 1 – Proposed converter and operating modes: a) schematic circuit of the proposed converter; b) Activation signals for the buck and boost switches; c) operating modes of the converter in both buck and boost operations.
Further, in order to provide the doubled ripple frequency in the inductor ripple current, the selected sequence of driving signals for the MDBBC switches are shown in Fig. 1b. In the proposed MDBBC the switching pattern for the switches is shifted by $360°/(p \times q)$, where ‘$p$’ is no. of phases in the converter and ‘$q$’ is no. of parallel switches and diodes per phase [31]. The input ripple current frequency is $(p \times q)$ times the switching frequency. Similarly, the switching frequency of the voltage ripples in filter capacitors is $(p \times q)$ times the switching frequency, which results in reduction of filter component sizes by ‘$q$’ times as that of conventional single switch buck-boost converter. In this proposed converter ‘$p$’ is chosen to be 1 and while ‘$q$’ is selected to be 2. Fig. 1c demonstrates the switching pattern sequence of the activation signals for the four operating modes. Further, the equivalent circuit diagrams under the four operating intervals based on the chosen switching pattern are illustrated in Fig. 2. Here, continuous conduction mode is assumed for the analysis of steady state behaviour of the converter. The switches $S_1$ and $S_2$ have identical duty cycles, i.e., $d_1 = d_2 = d_{12} = 0.1$ and $S_3$ and $S_4$ have the duty cycles of $d_3 = d_4 = d_{34} = 0.5$, where ‘$d$’ is the duty cycle.

Fig. 2 – Conduction diagrams of MDBBC for duty cycle $d_1 = d_2 = d_{12} = 0.1$ and $d_3 = d_4 = d_{34} = 0.5$: a) Conduction diagram for Mode I: $t_0 \leq t \leq t_1$; b) Conduction diagram for Mode II: $t_1 \leq t \leq t_2$; c) Conduction diagram for Mode III: $t_2 \leq t \leq t_3$; d) Conduction diagram for Mode IV: $t_3 \leq t \leq t_4$. 
3 Principle of Operation and Steady State Behaviour of the Proposed Converter

The proposed MDBBC converter is operated in both buck and boost modes of operation as shown in Figs. 3a and 3c, respectively. In boost operating mode the switches $S_1$ and $S_2$ are operated in PWM and $S_3$ and $S_4$ are continuously on in a half cycle with 50% duty cycle, similarly in the buck mode of operation switches $S_3$ and $S_4$ are operated in PWM while $S_1$ and $S_2$ remains off. The waveforms in Figs. 3b and 3d portray the steady state characteristics of MDBBC in both buck and boost operating modes respectively.

The duty cycles for the switches $S_1$ and $S_2$ are considered as $d_{12}(t)$ and for $S_3$ and $S_4$ it is $d_{34}(t)$. The duty cycles of the switches are adjusted to get the output voltage of around 36 V in both buck and boost modes of operation. In fuel cell applications it is necessary that the input ripple current must be lower than 5% of normal rated value to ensure the satisfactory FC operation [22, 23]. One can scrutinize the ripple percent in Figs. 3b and 3d as only less than 4% with the proposed converter.

Also the capacitor voltage ripple is less and lies between 0.2 and 0.4 V. The presence of oscillations in the output voltage at the boundary of operation is attenuated by placing a damping network at the middle of boost and buck circuits [15]. The benefit of using damping network in reducing output voltage oscillation is explained in [24] using the frequency and time domain analysis.

Moreover, employing the multi device technique in addition to the interleaving can further reduce the input current and voltage ripples, reduce converter size and increase efficiency and such buck-boost converters are best suitable for medium power applications. For elaborating the fundamental principles of operation and obtaining the state equations of the proposed converter in buck and boost operating modes the selected switching pattern is shown in the Fig. 3c.

The switching strategy chosen ensures all the possible switching states in a time period. In Mode I, $S_1$ and $S_3$ are conducting while $S_2$ and $S_4$ are switched off, in Mode II, $S_3$ is on and the remaining switches $S_1$, $S_2$ and $S_4$ are turned off, in Mode III, the switches $S_2$ and $S_4$ are conducting while $S_1$ and $S_3$ are turned off, in Mode IV, the switch $S_4$ is only turned on and remaining $S_1$, $S_2$ and $S_3$ are switched off.

The differential equations of the converter in both operating modes can be written by assuming the continuous conduction mode. In one time period there are four operating intervals available and further the corresponding equivalent circuit diagrams representing the voltage drops and current distribution at nodes are illustrated in Fig 4. Further, in order to obtain the differential equations the popular method called state space averaging method [2] is used. Similarly the other method called signal flow graph [25] can also be used for deriving the transfer functions to evaluate the dynamic performance of the converter.
The operating modes of the converter can be explained in four operating modes as follows:

**Mode I: \( t_0 \leq t \leq t_1 \):** At time \( t_0 \) the switches \( S_1 \) and \( S_3 \) are turned on, then the inductor \( L_1 \) starts storing energy in it. The stored energy in the inductor \( L_1 \) transfers to the load (as the switch \( S_3 \) is conducting, the input energy can reach output side through the path formed). The conduction path is demonstrated in the Fig. 2a. Further, the corresponding equivalent circuit is shown in the Fig. 4a and the inductor currents and capacitor voltage equations are shown in (1).

**Mode II: \( t_1 \leq t \leq t_2 \):** At time \( t_1 \) only \( S_3 \) is conducting while \( S_1, S_2 \) and \( S_4 \) are turned off, the energy emanated from the source reaches load through the conducting switch \( S_3 \) the energy transfers from source to load through the conduction path shown in Fig. 2b. The corresponding equivalent circuit is depicted in Fig. 4b. Here the capacitor \( C_1 \) supplies the demanded load current, whereas \( C_d \) charges. The set of differential equations for this mode similarly can be written as done in mode I. the related equations are presented in Appendix-I \((A_1)\).

\[
\begin{align*}
v_{l1}(t) &= L_1 \frac{di_{l1}(t)}{dt} = v_s(t) - v_{cl}(t), \\
v_{l2}(t) &= L_2 \frac{di_{l2}(t)}{dt} = v_{cd}(t) - v_o(t) \quad \text{or} \quad v_{cl}(t) - v_o(t), \\
i_{cl}(t) &= C_1 \frac{dv_{c2}(t)}{dt} = i_{l1}(t) - (i_{cd}(t) + i_{l2}(t)), \\
i_{cd}(t) &= C_d \frac{dv_{cd}(t)}{dt} = \frac{v_{cl}(t) - v_{cd}(t)}{R_d} = i_x(t) - i_{l2}(t), \\
i_x &= i_c(t) + i_{l2}(t) \quad \text{or} \quad i_{l1}(t) - i_{cl}(t), \\
i_{c2}(t) &= C_2 \frac{dv_{c2}(t)}{dt} = i_{l2}(t) - \frac{v_o(t)}{R_o}. 
\end{align*}
\]

**Mode III: \( t_2 \leq t \leq t_3 \):** At time \( t_2 \) the switches \( S_2 \) and \( S_4 \) are conducting while the other switches \( S_1 \) and \( S_3 \) are turned off, the energy emanated from the source appears at the load through the path as shown in Fig. 2c. The corresponding equivalent circuit is shown in Fig. 4c. The set of differential equations of voltage and current through the components are presented in Appendix \((A_2)\).

**Mode IV: \( t_3 \leq t \leq t_4 \):** At time \( t_3 \) only the switch \( S_4 \) is conducting while the other switches \( S_1, S_2 \) and \( S_3 \) are turned off, the energy transfers from source to load through the conduction path as shown in Fig. 2d. The corresponding equivalent circuit representing voltages and currents is shown in Fig. 4d. In this mode also the \( C_1 \) discharges to aid the supply current, the set of differential equations for this mode similarly can be written. It is presented in Appendix \((A_3)\).
After analysing the individual modes of operation with clear differential
equations, by applying SSA method to the converter model over a switching
period, one can write the modelling equations as shown in (2) While applying
this technique it is assumed that the circuit is operating in continuous
conduction mode, parasitic effects are neglected, and the switching frequency is
much higher than the converter’s usual frequencies. On applying the technique
following differential equations are obtained.
\[
L_1 \frac{d \bar{v}_c}{dt} = \bar{v}_s(t) - \bar{v}_c(1 - d_{12}(t)), \quad (2)
\]
\[
L_2 \frac{d \bar{v}_c}{dt} = \bar{v}_c(t)(1 - d_{12}(t)) - \bar{v}_o(t),
\]
\[
C_1 \frac{d \bar{v}_c}{dt} = \bar{L}_1(t)(1 - d_{12}(t)) - \bar{L}_2(t)(1 - d_{34}(t)) - \frac{\bar{v}_c(t) - \bar{v}_o(t)}{R_d},
\]
\[
C_d \frac{d \bar{v}_d}{dt} = -\frac{\bar{v}_d(t) + \bar{v}_c(t)}{R_d},
\]
\[
C_2 \frac{d \bar{v}_o}{dt} = \bar{L}_2(t) - \bar{v}_o(t).
\]

The accent over a signal stands for averaging done in a switching period.
\[d_{12}\] and \[d_{34}\] denotes that the duty cycles of the switches \[S_1, S_2\] and \[S_3, S_4\]
respectively. The circuit based analysis for obtaining (2) is carried out when we
replace with the time averaged models [26], which results in a large signal
model as shown in Fig. 5a assuming the converter operating under steady state
condition and the corresponding constant duty cycles are \[D_{12}\] and \[D_{34}\] and the
input voltage \[v_s(t) = V_s\], one can write expressions of capacitor voltages and
inductor currents by applying the inductor volte second balance and capacitor
charge balance under steady state condition [2]:
\[
I_s = I_{L1} = \frac{V_s \times D_{34}}{R_c(1 - D_{12})}, \quad I_o = I_{L2} - I_{C2} = \frac{V_o}{R_o},
\]
\[
V_{C1} = \frac{V_s}{(1 - D_{12})}, \quad V_{cd} = \frac{V_s}{(1 - D_{12})}, \quad V_o = \frac{V_s \times D_{34}}{(1 - D_{12})} = V_{C1} \times D_{34}.
\]

The steady state equation obtained in (3) can also be obtained by equating
the derivatives to zero in (2); the dc equivalent model representing the steady
state parameters is shown in Fig. 5b. From (3) a unified voltage conversion ratio
is defined as follows.
\[
K(D_{12}, D_{34}) = \frac{V_o}{V_s} = \frac{D_{34}}{(1 - D_{12})}.
\]
Fig. 3 – Equivalent circuit and key waveforms in buck and boost operating modes:
(a) Buck mode equivalent circuit; (b) Voltages and currents in buck mode with $V_s = 45 \text{ V}$ ($d_{34} = 0.4185$); (c) Boost mode equivalent circuit; (d) Voltages and currents in boost mode with $V_s = 28 \text{ V}$ ($d_{12} = 0.1388$).

The ultimate objective of the proposed converter is to operate in both buck ($0 < D_{34} < 1$ and $D_{12} = 0$) and boost ($0 < D_{12} < 1$ and $D_{34} = 0$) modes and that the transition from boost to buck and buck to boost modes must occur smoothly.

Let ‘u’ be the single control variable ranges from 0 to 2. The duty cycles can be re written as

$$D_{12} = \max(0, u - 1),$$  \hspace{1cm} (5)

$$D_{34} = \min(1, u).$$  \hspace{1cm} (6)

With the above consideration of single variable parameter the new voltage conversion ratio results as follows:
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\[ K(u) = \frac{\min(1, u)}{1 - \max(0, u - 1)} \]  \hspace{1cm} (7)

Using (7) smooth transition of DC voltage conversion ratio between buck and boost modes of operation can be easily achieved as illustrated in Fig. 5c.

\[ \begin{align*}
K(u) &= \frac{\min(1, u)}{1 - \max(0, u - 1)} \\
\text{Using (7) smooth transition of DC voltage conversion ratio between buck and boost modes of operation can be easily achieved as illustrated in Fig. 5c.}
\end{align*} \]

\[ \begin{align*}
(a) & \quad \begin{align*}
& h_1 \quad L_1 \\
& v_i \quad i_{d1} \quad i_{d2} \quad i_{d3} \\
& v_o \\
& R_d \\
& C_1 \\
& S_{ON} \\
\end{align*} \\
& \text{Fig. 4 – Equivalent circuit diagrams of proposed converter for duty cycle } d_{12} = 0.1 \\
& \text{and } d_{34} = 0.5: a) \text{ Electrical equivalent circuit diagram for Mode I: } t_0 \leq t \leq t_1; \\
& b) \text{ Electrical equivalent circuit diagram for Mode II: } t_1 \leq t \leq t_2; \\
& c) \text{ Electrical equivalent circuit diagram for Mode III: } t_2 \leq t \leq t_3; \\
& d) \text{ Electrical equivalent circuit diagram for Mode IV: } t_3 \leq t \leq t_4.
\end{align*} \]

\[ \begin{align*}
(b) & \quad \begin{align*}
& h_1 \quad L_1 \\
& v_i \quad i_{d1} \quad i_{d2} \quad i_{d3} \\
& v_o \\
& R_d \\
& C_1 \\
& S_{ON} \\
\end{align*} \\
& \text{Fig. 5a – Circuit model of the MDBBC with damping network and DC conversion ratio: a) Equivalent averaged model for large signal analysis;}
\end{align*} \]
4 Design Guidelines

The proposed MDBBC is designed as the battery charging/discharging regulator for the 36 V battery bank series, whose design specifications are shown in the Table 1. The input voltage ranges from 28 to 45 V and the regulated output voltage is around 36 V. A low ripple current on the input side is the key requirement, and the inductors play major role in reducing the ripple, hence a suitable value of inductance has to be chosen. The current ripple in the both buck and boost side inductors $\Delta i_{L1}$ and $\Delta i_{L2}$ is limited to 0.4 A, and then according to that the necessary value of inductance is determined using the equations presented in Table 2. Similarly the filter capacitors on both sides are chosen by defining the voltage ripples $\Delta v_{c1}$ and $\Delta v_{c2}$ to be maximum 0.2 V, and accordingly the capacitor values are selected.
Table 1

<table>
<thead>
<tr>
<th>Parameter/Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>28-45 (suits for FCS1000)</td>
</tr>
<tr>
<td>Output voltage</td>
<td>36 V</td>
</tr>
<tr>
<td>Maximum output power</td>
<td>270 W</td>
</tr>
<tr>
<td>Load resistance</td>
<td>4.8 Ω</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>50 kHz</td>
</tr>
<tr>
<td>Input ripple- peak-peak</td>
<td>0.4 A</td>
</tr>
<tr>
<td>Capacitor voltage ripple</td>
<td>0.2 V</td>
</tr>
<tr>
<td>Power loss in the damping resistor</td>
<td>1 W</td>
</tr>
</tbody>
</table>

The multi device operation of buck-boost converter helps in using the smaller inductor for reduced ripple current; the inductor value gets reduced by ‘q’ times as that of conventional BBC, where q is equal to 2 for MDBBC. As discussed in the introduction part about the non-minimum phase system, to overcome this problem a RC damping network is connected at the boundary between buck and boost operating modes. The derived expressions used for selecting these values are presented in Table 2 as well. After performing the suitable analyses in both buck and boost modes of operation of MDBBC, the finalized list of components are presented in Table 3.

Table 2

Necessary equations to determine the parameters of MDBBC.

<table>
<thead>
<tr>
<th>Buck mode</th>
<th>Boost mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_2 = \frac{(V_s - V_o)V_o}{q \times V_s \times \Delta i_{L2_p-k_p}} \times T_s$</td>
<td>$L_1 = \frac{(V_o - V_s)V_s}{q \times V_o \times \Delta i_{L1_p-k_p}} \times T_s$</td>
</tr>
<tr>
<td>$C_2 = \frac{(V_s - V_o)V_o^2}{q \times R \times V_s^2 \times \Delta v_{C2_p-k_p}} \times T_s$</td>
<td>$C_1 = \frac{(V_o - V_s)V_s^2}{q \times R \times V_s^2 \times \Delta v_{C1_p-k_p}} \times T_s$</td>
</tr>
<tr>
<td>$C_d &gt; 8C_1$, $R_d &gt; 0.65 \sqrt{\frac{L_1}{C_1}}$</td>
<td></td>
</tr>
</tbody>
</table>

During buck mode of operation of MDBBC, the passive component parameters are selected based on the following parameters

Input voltage of the converter $V_s = 45$ V, Output voltage of the converter $V_o = 36$ V, No. of devices/phase ‘q’ = 2, allowed ripple current in buck inductor $\Delta i_{L2_p-k_p} = 0.6$ A, allowed ripple voltage in output capacitor or buck capacitor...
\( \Delta V_{c2 \text{ pk-pk}} = 0.2 \text{ V} \), Switching frequency \( F_s = 50 \text{ kHz} \). Time period for one cycle \( T_s = 1/50 \text{ kHz} = 20 \mu\text{s} \).

The passive component values are calculated using the relations given in Table 2. The buck inductance \( L_2 \) and capacitance \( C_2 \) are calculated as:

\[
L_2 = \frac{(45 - 36)36}{2 \times 45 \times 0.6} \times 20 \times 10^{-6}, \quad C_2 = \frac{(45 - 36)36^2}{2 \times 4.8 \times 45^2 \times 0.2} \times 20 \times 10^{-6},
\]

\[ L_2 = 120 \mu\text{H}, \quad C_2 = 60 \mu\text{F}. \]

The practical values of the components connected in circuit are \( L_2 = 120 \mu\text{H} \) and \( C_2 = 68 \mu\text{F} \) (next higher rating available in market). Also the ripple current in the buck inductor is not considered as important as that of the ripple current in boost inductor, because the load current ripple with 8% is considerable.

During boost mode of operation the passive component parameters are chosen by the following calculations.

Input voltage of the converter \( V_s = 28 \text{ V} \), Output voltage of the converter \( V_o = 36 \text{ V} \), No. of devices/phase ’q’ = 2, allowed ripple current in buck inductor \( \Delta i_{L2 \text{ pk-pk}} = 0.4 \text{ A} \), allowed ripple voltage in output capacitor or buck capacitor \( \Delta V_{c2 \text{ pk-pk}} = 0.35 \text{ V} \), Switching frequency \( F_s = 50 \text{ kHz} \), Time period for one cycle \( T_s = 1/50 \text{ kHz} = 20 \mu\text{s} \).

The passive component values are calculated using the relations given in Table 2. The buck inductance \( L_1 \) and capacitance \( C_1 \) are calculated as:

\[
L_1 = \frac{(36 - 28)28}{2 \times 36 \times 0.4} \times 20 \times 10^{-6}, \quad C_1 = \frac{(36 - 28)28^2}{2 \times 4.8 \times 36^2 \times 0.35} \times 20 \times 10^{-6},
\]

\[ L_1 = 155 \mu\text{H}, \quad L_1 = 28.8 \mu\text{F}. \]

Apart from the passive components, the damping resistor and capacitor values are chosen based on the condition that the \( C_d \) should be greater than eight times of the boost inductor, i.e., \( 8 \times 47 \mu\text{F} = 376 \mu\text{F} \). Here in the prototype model a capacitor value of 470 \( \mu\text{F} \). The damping resistor value as given in the Table 2 value is chosen as 1 Ohm and around 1 W of heat dissipates in it.

The N-channel MOSFETS with low on-state resistance is considered to achieve good efficiency, and to ensure the faster operation Schottkey diodes are preferred. The inductors are of handmade, the buck side inductor \( L_2 \) has to carry 7.5 A and hence SWG 14 wire size is chosen as it can carry a maximum current of 9.3A, whereas on boost side the maximum current flow is 10 A and hence SWG 13 wire is selected as it can carry 12 A easily. Available laboratory type DC voltage sources in conventional lab are not capable of delivering more than 7 A, but the peak current supply requirement is of 10 A under the boost operating mode of the converter, for which a single phase bridge rectifier is preferred to get the required DC voltages for experimentation and measuring of the efficiency.
5 Simulation Study

The proposed converter model is developed and studied on the Matlab/Simulink platform as shown in Fig. 7. All the component values are shown in Table 3.

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1, S_2, S_3, S_4$</td>
<td>Power MOSFETs</td>
<td>IRFZ44N</td>
</tr>
<tr>
<td>$D_1, D_2, D_3, D_4$</td>
<td>Schottkey diodes</td>
<td>MBR14100</td>
</tr>
<tr>
<td>$L_1$</td>
<td>Boost inductor</td>
<td>Wire size: SWG 13&lt;br&gt;Core type: Soft ferrite&lt;br&gt;No of turns: 20&lt;br&gt;160 $\mu$H</td>
</tr>
<tr>
<td>$L_2$</td>
<td>Buck inductor</td>
<td>Wire size: SWG 14&lt;br&gt;Core type: Soft ferrite&lt;br&gt;No of turns: 15&lt;br&gt;120 $\mu$H</td>
</tr>
<tr>
<td>$C_1$</td>
<td>Ceramic capacitors</td>
<td>47 $\mu$F, 63 V</td>
</tr>
<tr>
<td>$C_d$</td>
<td>Damping capacitor</td>
<td>470 $\mu$F, 63 V</td>
</tr>
<tr>
<td>$R_d$</td>
<td>Damping Resistor</td>
<td>1 $\Omega$, 1 W</td>
</tr>
<tr>
<td>$C_2$</td>
<td>Output capacitor</td>
<td>68 $\mu$F, 100 V</td>
</tr>
</tbody>
</table>

The converter is operated individually in buck and boost operating modes. When operated in buck mode the boost switches $S_1$ and $S_2$ are turned off and buck switches $S_3$ and $S_4$ are operated in PWM. On the other hand when the converter is operated in boost mode the buck switches are permanently on and the boost switches are operated in PWM. The PWM pulses for the switches are adjusted to get $v_o = 36$ V, this is achieved in buck mode for the duty cycle of $d_{34} = 0.4185$, being the source voltage fixed at 45 V. In boost operating $d_{12} = 0.1388$ for the input voltage of 28 V. As the on time is reduced, the switch conducts for lesser time, reducing the switch conduction. This helps in transferring more input energy to load, thereby increasing efficiency.

Figs. 3b and 3d illustrate the activation signals for buck and boost switches respectively. In order to get voltage regulation the converter can be operated in closed loop voltage controlled mode by a PI controller. Figs. 6a and 6b show the ripples in output inductor current, output current, output voltage and boost capacitor voltage for $v_s = 45$ V and $v_s = 40$ V respectively, which it is observed that for reduced input voltage the inductor ripple current is also reduced by a significant value, it is to be noted that the ripples in input side current during buck mode is very small and one can observe in Fig. 3b.
Fig. 6 – Voltage and current waveforms with ripple in buck and boost operating modes:
a) Ripples in current and voltage in buck mode for $V_s = 45$ V;
b) Ripples in current and voltage in buck mode for $V_s = 40$ V;
c) Ripples in I/O current, capacitor voltage and output voltage in boost mode for $V_s = 28$ V; d) Ripples in I/O current, capacitor voltage and output voltage in boost mode for $V_s = 32$ V.

Fig. 7 – MATLAB Simulation model of the proposed converter.
Similarly in boost operating mode for two different input voltages \( v_s = 28 \, \text{V} \) and \( v_s = 32 \, \text{V} \), the ripples in input current \( (I_{L1}) \), output current \( (I_o) \) output voltage \( (V_o) \) and capacitor \( C_1 \) voltage \( (V_{c1}) \) are shown in Figs. 6b and 6d.

6 Experimental Results

The proposed MDBBC circuit model is designed to provide an output voltage of 36 V when its source voltage varies from 28 to 45 V. The experimental setup and prototype model is shown in in Fig. 8. The maximum power is restricted to 270 W \((36\,\text{V} \times 7.5\,\text{A})\) or \((7.5\,\text{W} \times 4.8\,\Omega)\) and the corresponding load resistance is 4.8 \( \Omega \). The duty cycles for the buck mode is in the range of \( 0.4185 < D_{b1} < 1 \) and for boost mode is \( 0 < D_{b1} < 0.1388 \). The switching frequency is selected to be of 50 kHz, as this is the optimum frequency level which is observed for the proposed converter. The frequency over the 50 kHz introduces additional switching and conduction losses but the passive components sizes get reduced, the increased losses leads to the less energy efficient system. Choosing below the 50 kHz is also not feasible requires large size passive components and hence it is selected based on the trade-off among the power losses, size of passive components and EMI interference.

Further the inductor ripple current and capacitor voltage ripple are selected to be of 0.4 A and 0.2 V respectively, provided the passive components to be of less value as shown in Table 3. The proposed converter can be best suitable as FC voltage regulation system to meet the practical application as voltage regulator for a Horizon PEM fuel cell model “H-1000-FCS-C1000”. Its voltage varies from 28 to 45 V full load to no load. The output voltage of this FC is unregulated and it has to be regulated to get 36 V constant values for the purpose of charging a 36V battery bank. The components are designed based on the expressions and aforementioned ripple as shown in Table 2 and Table 1.

To obtain the real time switching signals for the buck and boost switches an “Altium3000NB” FPGA controller has been used. A triangle shaped carrier wave is compared with the reference DC voltage to produce the firing pulses by using Xilinx Spartan ISE 14.1 system generator, which can convert the PWM logic into high speed VHDL code. The generated code is dumped into the “Altium3000NB FPGA”. Further the generated pulses from the FPGA ports are given to the driver circuits of the switches. The key experimental waveforms are obtained on the DSO.

The waveforms illustrated here are of gating pulses for the switches as shown in Figs. 9a, 9b and 9c show the ripple current on the input side during the boost operation mode, because the key point of interest is the reduction of ripple current. The ripple current observed is close to the simulation results shown in the Figs. 6c and 6d, being 4%, which is highly appreciable for fuel cell applications. The previous reported value of the input ripple current by several authors are 5.2% in [20] and 9.2% in [30], 23% in [29], 28% in [19], 32% in [15], and 33% in [28].
For any power converter the energy conversion efficiency is an important consideration, the proposed converter efficiency is determined by experimental setup which includes power analyser and dc electronic load, the measured efficiency includes the control stages and driver stage power losses, calibrated shunt resistors are used to measure the currents on input and output side. Fig. 10 shows the overall system efficiency as a function of load or output current $i_o$ for different source voltage levels and the variation of efficiency is plotted for different output currents and source voltage as reference on the horizontal axis. One can see from the efficiency plot that the maximum efficacy occurs at the end of the buck mode of operation, i.e., $v_s = 42 \text{ V} – 44 \text{ V}$.

![Fig. 8 – Experimental setup and power circuit of MDBBC: a) Experimental setup; b) Power circuit.](image)
Fig. 9 – Experimental results of MDBBC prototype converter model:

a) Switching activation signals for buck and boost mode switches;

b) Input source current or inductor ($L_1$) current and output load current ripples in boost operating mode for $V_s = 28$ V;

c) Input source current or inductor ($L_1$) current and output load current ripples in boost operating mode for $V_s = 32$ V.

Fig. 10 – Measured efficiency of the proposed MDBBC for $V_o = 36$ V.
It can also be seen from energy efficiency plot that when the converter is operating in the buck stage, the efficiency obtained is higher compared to the boost stage, the reason for this is the boost switches are off during the buck mode of operation, and hence the power losses reduce. Thus such high value of efficiency with hard switching operation proves that the proposed converter is best suitable for low voltage applications. The overall maximum power stage losses which occur in the process of operation are of 18 W with inclusion of power losses in the inductor. These losses can be further reduced by employing some zero voltage switching, multi device interleaving operation.

7 Conclusion

A new non inverting multi device buck-boost dc-dc converter suitable for fuel cell low voltage applications has been introduced in this paper. The designed MDBBC operates either in buck or boost CCM mode and the converter behaviour under steady state operation are presented. The converter efficiently operates in buck and boost operating modes, when operating in buck mode the boost switches are off whereas in boost operation the buck switches are permanently on. The placement of an intermediate damping network between the buck and boost operating modes reduces the damping oscillation in the output voltage under boundary operation. Further the basic circuit operation of proposed converter, design procedures and selection of key components were clearly described with neat diagrams. Moreover the $s$ domain model and analysis of converter differential equations are derived.

A high efficiency is obtained under the three operating modes of operation including buck, boost and boundary region operation, based on the I/O voltage ratio factor. It has been experimentally verified that the proposed MDBBC has peak and average efficiency of 97.68% and 96.25% respectively, which can be further improved by ZVS or multi device interleaving operation on the boost side or input side of the converter. The designed converter is best suitable for the applications such as FC devices for battery charging because it has the ripple current less than the permissible value as 5% and other applications such as PV panels, super capacitors and other low voltage applications also can use this topology. Further, operating the converter in buck-boost mode results in a non-minimum phase system as there is presence of RHP zeros on the $s$-plane, research yet to carry to overcome the drawback of non-minimum phase system.

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9 Appendix

In this appendix the differential equations of capacitor voltages and currents for the equivalent circuits shown in Figs. 4c – 4d.

(b) Mode II: $t_1 \leq t \leq t_2$, Fig. 4b

\[ v_{L1}(t) = L_1 \frac{di_{L1}(t)}{dt} = v_s(t) - v_{c1}(t), \]
\[ v_{L2}(t) = L_2 \frac{di_{L2}(t)}{dt} = v_{cd}(t) - v_o(t) or v_{c1}(t) - v_o(t), \]
\[ i_{c1}(t) = C_1 \frac{dv_{c1}(t)}{dt} = i_{L1}(t) - (i_{cd}(t) + i_{L2}(t)) or v_{c1}(t) - i_y(t), \]
\[ i_{cd}(t) = C_d \frac{dv_{c2}(t)}{dt} = \frac{v_{c1}(t) - v_{cd}(t)}{R_d} = i_y(t) - i_{L2}(t). \]

Here $i_y$ is transition mode current, the current between two operating modes:

\[ i_y = i_{cd}(t) + i_{L2}(t) \quad or \quad i_{c1}(t) + i_{L1}(t), \]
\[ i_{c2}(t) = C_2 \frac{dv_{C2}(t)}{dt} = i_{L2}(t) - \frac{v_o(t)}{R_o}. \]

(c) Mode III: $t_2 \leq t \leq t_3$, Fig. 4c

\[ v_{L1}(t) = L_1 \frac{di_{L1}(t)}{dt} = v_s(t) - v_{c1}(t), \]
\[ v_{L2}(t) = L_2 \frac{di_{L2}(t)}{dt} = v_{cd}(t) - v_o(t) \quad or \quad v_{c1}(t) - v_o(t), \]
\[ i_{c1}(t) = C_1 \frac{dv_{c1}(t)}{dt} = i_{L1}(t) - (i_{cd}(t) + i_{L2}(t)), \]
\[ i_{cd}(t) = C_d \frac{dv_{c2}(t)}{dt} = \frac{v_{c1}(t) - v_{cd}(t)}{R_d} = i_x(t) - i_{L2}(t). \]

Here $i_x$ is transition mode current, the current between two operating modes:

\[ i_x = i_c(t) + i_{L2}(t) \quad or \quad i_{L1}(t) - i_{c1}(t), \]
\[ i_{c2}(t) = C_2 \frac{dv_{C2}(t)}{dt} = i_{L2}(t) - \frac{v_o(t)}{R_o}. \]
(d) **Mode IV**: $t_3 \leq t \leq t_4$, Fig. 4d

\[
\begin{align*}
    v_{L1}(t) &= L_1 \frac{di_{L1}(t)}{dt} = v_s(t) - v_{c1}(t), \\
    v_{L2}(t) &= L_2 \frac{di_{L2}(t)}{dt} = v_{cd}(t) - v_o(t) \quad \text{or} \quad v_{c1}(t) - v_o(t), \\
    i_{c1}(t) &= C_1 \frac{dv_{c1}(t)}{dt} = i_{L1}(t) - (i_{cd}(t) + i_{L2}(t)) \quad \text{or} \quad i_{L1}(t) - i_y(t), \\
    i_{cd}(t) &= C_d \frac{dv_{cd}(t)}{dt} = \frac{v_{c1}(t) - v_{cd}(t)}{R_d}(t) = i_y(t) - i_{L2}(t).
\end{align*}
\]

(A3)

Here $i_y$ is transition mode current, the current between two operating modes:

\[
i_y = i_{cd}(t) + i_{L2}(t) \quad \text{or} \quad i_{c1}(t) + i_{L1}(t)
\]

\[
i_{c2}(t) = C_2 \frac{dv_{c2}(t)}{dt} = i_{L2}(t) - \frac{v_o(t)}{R_o}.
\]

### 10 References


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