

Design of Low-Temperature DDOAs on the Elements of BiJFet Array Chip MH2XA030

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Abstract: Brief information about the new BiJFet array chip (AC) MH2XA030 intended for accelerated creation of analog integrated circuits (IC), which retain their performance under the influence of penetrating radiation and extremely low temperatures (up to minus 197 °C) is presented. The features of schematic design of two types of DDOAs (OAmpl3, OAmpl4) are considered. The recommendations on the schematic design of the DDOA are developed taking into account the static characteristics of the field effect and bipolar transistors of the AC under the influence of low temperatures. The amplitude-frequency response of the DDOA and the dependence of the noise voltage on the frequency of Fourier density are given. At a temperature of –197°C cryogenic amplifiers OAmpl3 (OAmpl4) are characterized by the following parameters: the current consumption is less than 500 µA, the input current is less than 1 fA, the voltage gain is more than 50.000 (200.000), the offset voltage is less than 200 (60) µV. The results of the circuit simulation of the instrumentation amplifier based on DDOA OAmpl3 are presented.

Keywords: Analog integrated circuits, Array chip, Radiation hardness, Cryogenic electronics, Differential difference operational amplifier.

1 Introduction

Analog integrated circuits (IC) have a significant effect on the static and dynamic parameters of automation devices, measuring equipment, instrumentation and telecommunications [1 – 3]. Differential difference operational amplifier (DDOA) is a relatively new functional node of analog circuitry which enables in some cases to obtain the parameters of analog devices that are unattainable when using classical op-amps [4]. In this regard, the improvement of the schematic design of the DDOA and its application in analog interfaces are given

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much attention [4 – 21]. Analog Devices, Texas Instruments, etc. are engaged in serial production of the DDOA for the problems of space instrument making [22, 23]. In this regard, we should note the relevance of the research of the DDOA for severe operation conditions [22].

Recently, we have carried out the studies both on the development of radiation-hardened structured arrays (SA) and array chips (AC) [23 – 26], and on the creation of a complex of design tools for cryogenic analog ICs [27, 28].

On the base of the results obtained the new AC MH2XA030 (in 2018) has been designed for accelerated design and low-volume production of the radiation-hardened and cryogenic analog ICs.

The purpose of the article is to consider the means and rules for schematic design of cryogenic analog ICs on the elements of the BiJFet AC MH2XA030, as well as the circuitry features of the developed DDOAs and the results of their simulation.

Section 2 describes the process of designing analog circuits on AC MH2XA030. Section 3 gives recommendations for circuit design of DDOA on the elements of AC. Section 4 shows the circuitry of DDOAs Oamp3 and Oamp4 to cryogenic temperatures. Section 5 shows the circuit of connection DDOA Oamp3 in the form of an instrument amplifier.

2 Design of the Chips on the AC MH2XA030

The AC MH2XA030 contains eight macrocells. On the perimeter of the AC there are complex functional bond sites (122 pcs.), which are used to connect the semiconductor element with conductors to the traverses of the package or as the following active elements: PADN - two multi-emitter high-power n-p-n-transistor; PADP - two multi-emitter high-power p-n-p transistors; PADJ - low-noise field effect transistor with p-n-junction and p-type channel (p-JFET). In total, 64 powerful n-p-n transistors, 60 powerful p-n-p transistors and 60 low-noise p-JFETs are located on the AC. The combined resistance of all AC resistors is 14.64 M Ω , and the total capacitance of all capacitors is 136.96 pF.

It is known [23] that not all commercial CAD systems and firm libraries of Spice parameters of transistor models are suitable for circuit simulation of the simultaneous effect of penetrating radiation and cryogenic temperature on the parameters of analog ICs. For the simultaneous consideration of the effect of radiation and low temperatures, it was proposed to use CAD LTSpice, built-in LTSpice standard models with averaged temperature coefficients, as well as the developed mathematical expressions that establish the relationship between the parameters of models, semiconductor and radiation exposure and describe a nonmonotonic change in the BETA p-JFET parameter [23, 25].

To identify the parameters of the models, we studied the main current-voltage characteristics (CVC) of the BJT and JFET at the temperature T up to -197°C , as well as under the influence of gamma radiation and the flux of fast electrons.

The low-temperature measurements are carried out on the experimental setup, given in Fig. 1 [29, 30]. The measured transistors are located in a metal glass, placed in the liquid nitrogen with the help of a rod with a wire harness of twisted pairs inside for connection of the semiconductor units to the tester IPPP-1. The measured data are delivered to the personal computer (PC) through the RS-232 interface.

The thermocouple of M type, defined in the Standard-P 8.585–2001 (Coper/Copel), is used to control the temperature. It is located close to the measured transistors. The temperature is registered by the “cold junction compensation” technique, at which an exposed end of the thermocouple is placed in the glass with water and floating ice (in Fig. 1 it is marked as a “glass of ice water”). The thermal EMF of the thermocouple is fixed by the voltmeter B7-65 and is delivered to the PC through the RS-232 interface. The measurements are carried out in the automatic mode under the control of the program in “VEE Pro” graphical language environment.

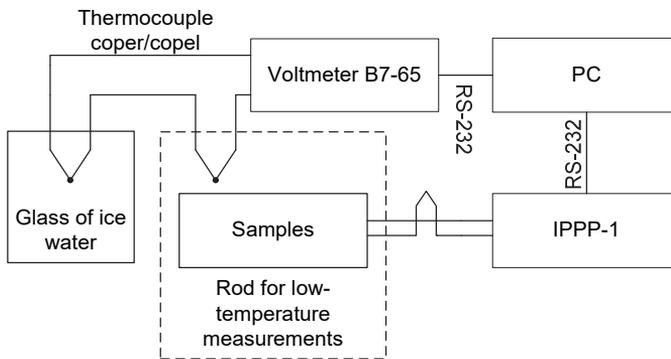


Fig. 1 – The circuit of the experimental setup for the low-temperature measurements.

Radiation change in CVC of the BJT and JFET was studied with the help of [31]:

- Linear electron accelerator ELU-4, providing a nominal electron energy of 4 MeV;
- Irradiation of samples with ^{60}Co gamma quanta at the “Researcher” installation with gamma radiation dose rate of (15 – 20) rad/s.

Irradiation of the samples was carried out at a temperature of about 300 K ($T = 27^{\circ}\text{C}$). The transistors were in active mode during irradiation.

Measurements of CVC transistors were performed using instruments and programs that were used in low temperature studies.

Based on the experimental data obtained (Figs. 2 – 6), transistor models were modified to simultaneously account for the effect of low temperatures and penetrating radiation [26].

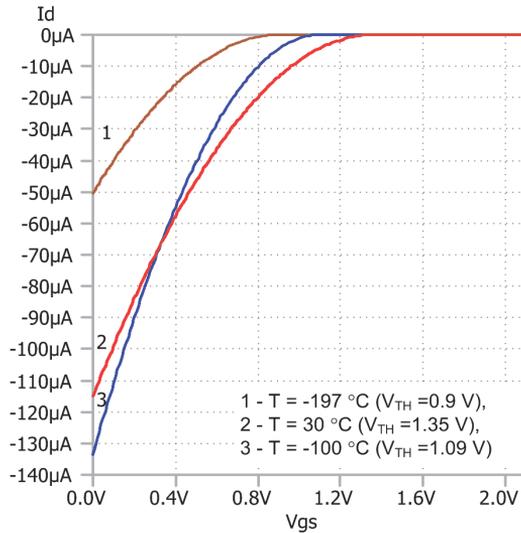


Fig. 2 – Dependence of the I_D on the V_{GS} of the low-power p-JFET AC with the minimum permissible cutoff at $V_{SD} = 3\text{ V}$ and different temperatures.

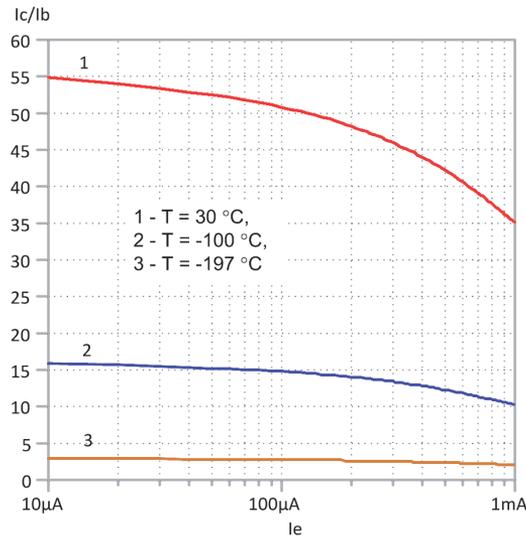


Fig. 3 – Dependence of the β of the low-power p-n-p transistor AC on the emitter current at different temperatures.

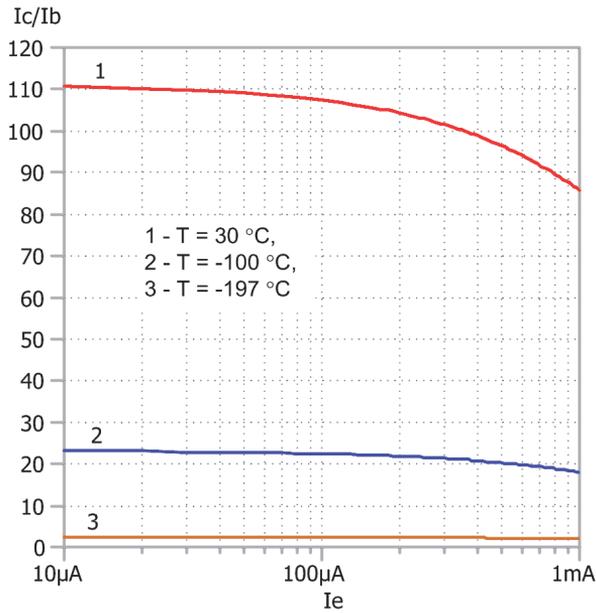


Fig. 4 – Dependence of the β of the low-power n - p - n -transistor CA on the emitter current at different temperatures.

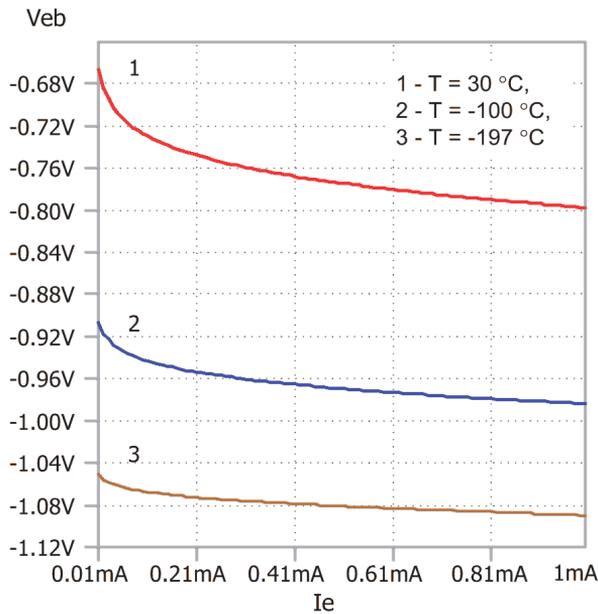


Fig. 5 – Dependence of the voltage on the forward-biased base-emitter junction V_{EB} of the low-power n - p - n -transistor AC on the emitter current at different temperatures.

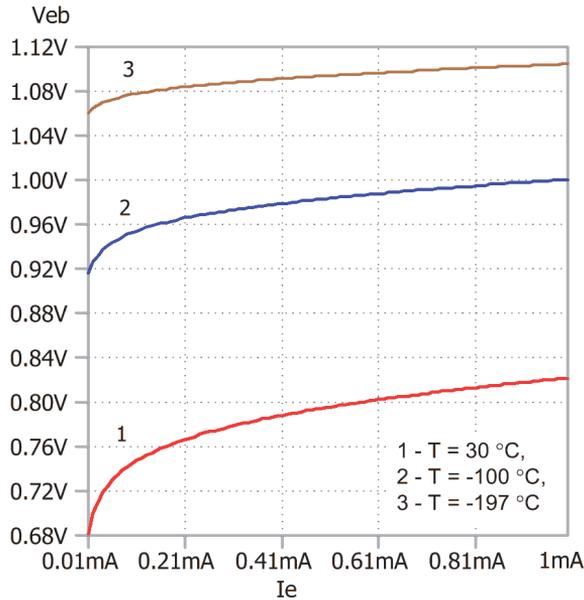


Fig. 6 – Dependence of the voltage on the forward-biased base-emitter junction V_{EB} of the low-power p-n-p-transistor AC on the emitter current at different temperatures.

The developed models enable us to describe the existing manufacturing tolerance of the cutoff voltage V_{TH} by changing the parameter VTOValue, the spread of the β – by changing the BFscale parameter, the effect of the absorbed dose of gamma radiation and the neutron flux by parameters of the D_G and F_N model, respectively. The use of these means ensured satisfactory coincidence of the results of measurement and simulation of CVC of the BJT and JFET at the temperature T up to -197°C [26].

Simulation of the CVC of the BJT and JFET, with simultaneous exposure to low temperatures and penetrating radiation, made it possible to establish that bipolar transistors retain a minimum operability ($\beta \geq 2$) in a small range of simultaneous external factors: $T = -197\text{ }^\circ\text{C}$, $F_N < 10^{12}\text{ n./cm}^2$, $D_G < 200\text{ krad}$. In connection with this, it can be recommended to develop either low-temperature schemes with low radiation resistance level or radiation-resistant circuits for $T > -60^\circ\text{C}$ on AC MH2XA030.

The analysis of the I-V characteristic shown in Figs. 2 – 6, and the cryogenic analog IC design recommendations formulated on its basis are considered in Section 3.

3 Recommendations for the Schematic Design of the DDOA on the AC Elements

When developing the cryogenic DDOAs, it is advisable to take into account the need to provide a large range of input signal, at which the transconductance of the input transistors varies slightly [21, 28], as well as the following recommendations that allow describing the existing technological dispersion of the parameters of bipolar and field effect transistors in the temperature range in the case of circuit simulation, which is especially important in the practical development of analog ICs, taking into account the limitations of the technological routes of specific manufacturers of semiconductor products.

First of all, before the beginning of the schematic synthesis of the DDOAs containing field effect and bipolar transistors, it is recommended to perform the simulation and analysis of dependencies: $I_D = f(V_{GS})$ at $V_{SD} = \text{const} \geq V_{TH}$; $\beta = f(I_E)$ at $V_{CB} = 1V$; the voltage on the forward-biased base-emitter junction $V_{EB} = f(I_E)$ at $V_{CB} = 1V$.

Simulation of the characteristics should be carried out under the following conditions:

- the permissible manufacturing tolerance of the cut-off voltage due to the measurement of the parameter $V_{TOValue} = 1.3; 1.44; 1.925$, which corresponds to $V_{TH} = 1.35 V; 1.5 V; 2 V$;
- the admissible manufacturing tolerance of the β ($BF_{scale} = 0.75, 1, 1.25$);
- in the temperature range up to $-197^\circ C$.

Studying the simulation results of the CVC of transistors makes it possible to identify the problems that can arise in the schematic synthesis of the DDOA. Thus:

- the cutoff voltage V_{TH} is significantly reduced at $T = -197^\circ C$. If under normal conditions the cutoff voltage corresponds to the minimum permissible value $V_{TH} = 1.35 V$, then at $T = -197^\circ C$ and it decreases up to $V_{TH} = 0.9 V$;
- the absolute value of the voltage on the forward-biased base-emitter junction at $T = -197^\circ C$ increases and may exceed the value of V_{TH} , and the β significantly decreases. For example, with $I_E = 50 \mu A$ for the n-p-n transistor $|V_{EB}|$ increases from $0.688 V$ under normal conditions up to $1.057 V$ at $T = -197^\circ C$, and the β falls from 110 to 2.39 , for the p-n-p transistor $|V_{EB}|$ increases from $0.704 V$ under normal conditions up to $1.066 V$ at $T = -197^\circ C$, and the β falls from 54 up to 2.83 . Therefore, in order to ensure the operability of the DDOA schemes with the permissible manufacturing tolerance of the V_{TH} , it is not necessary to

apply the connection of the emitter junctions between the source and the gate of the p-JFET. An alternative solution to this problem is to increase the V_{TH} norm under normal conditions, taking into account the drop in the cutoff voltage at extremely low temperatures;

- in cascades on bipolar transistors it is possible to compensate partially the sharp drop of the β due to the use of the circuits of the composite transistors (Fig. 7, Q10, Q8, Q1 и Q9, Q2, Q11).

4 Circuitry of the DDOA for Cryogenic Temperatures

Fig. 7 presents the electrical circuit of cryogenic DDOA OAm3, designed with the available AC MH2XA030 transistors and passive elements ratings.

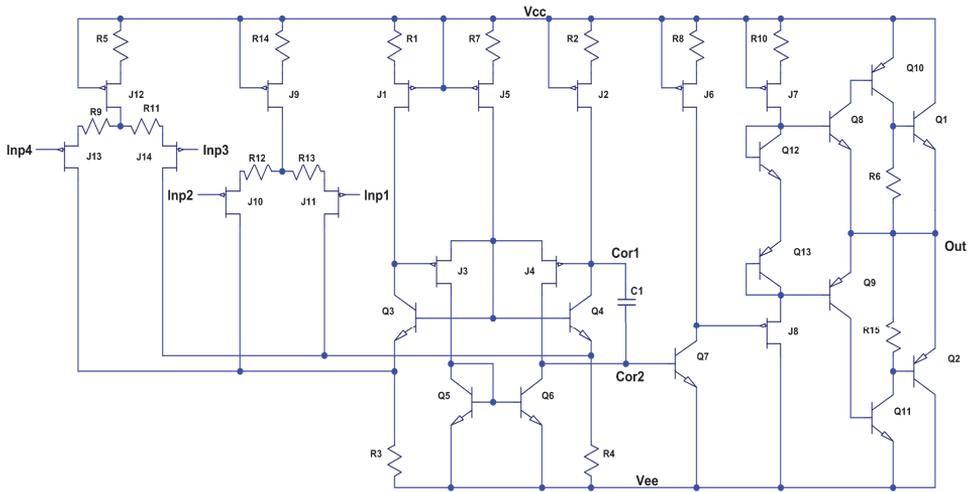


Fig. 7 – *Electrical circuit of cryogenic DDOA OAm3.*

The OAm3 is an upgrade of the low-temperature op amp [24] and includes three amplifying stages. Two classical input differential stages (DS) on field effect transistors J10, J11 and J13, J14 are connected in parallel, their output currents (drain currents J10, J11 and J13, J14) are summed on emitter resistors R3, R4 of common base transistors Q3, Q4. Thus, the input DS and transistors Q3, Q4 with an active load on the p-JFET J1, J2 form the first amplification stage, made in accordance with the “folded” cascode scheme.

The second amplification stage is a DS on p-JFET J3, J4 with a load in the form of “current mirror” Q5, Q6, and the third amplification stage includes transistor Q7 with a common emitter and an active load on p-JFET J6. Source follower J8, forward-biased diodes Q12, Q13, current source J7, emitter

followers on first (Q8, Q10, Q1) and second (Q9, Q11, Q2) composite transistors form a push-pull output stage.

The combination of the elements in the composite transistors provides a high value of their total gain $\beta_{\Sigma 1} \approx \beta_1 \cdot \beta_8 \cdot \beta_{10}$, $\beta_{\Sigma 2} \approx \beta_2 \cdot \beta_9 \cdot \beta_{11}$ and a relatively small voltage drop on the direct-switched emitter junction of the composite transistor $V_{EB\Sigma 1} = V_{EB8}$, $V_{EB\Sigma 2} = V_{EB9}$ in comparison with the typical scheme of Darlington transistor.

Resistors R6, R15 resistances are selected so that the output transistors Q1, Q2 do not open at $T = -197^\circ\text{C}$ and the small collector current Q10, Q11, for example, $R_6 \approx V_{EB1} / I_{C10\text{MIN}} \approx 1\text{V} / 10\mu\text{A} = 100\text{k}\Omega$. This reduces the current consumption of the output stage.

The operating modes of the transistors are chosen from the condition of minimizing the current consumption ($I_{R1} = I_{R2} = I_{R8} = 11.8\mu\text{A}$, $I_{R7} = 23.8\mu\text{A}$, $I_{R10} = 97.0\mu\text{A}$) and current sources J12, R5 and J9, R14 ($I_{R5} = I_{R14} = 100.9\mu\text{A}$) – for maximum increasing the linear operation range of the input DSs.

The operation of the DDOA without negative feedback circuits (NFC) explains the simulation results of the amplitude and phase frequency responses, Fig. 8.

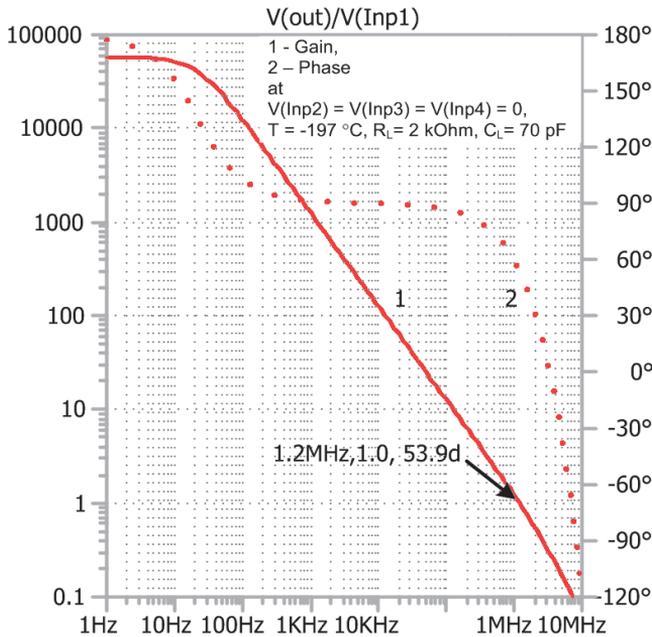


Fig. 8 – Dependence of the amplification gain and its phase of DDOA OAmP3 on the frequency at $T = -197^\circ\text{C}$.

Frequency correction of the DDOA is carried out by connection of a capacitor with a capacitance of 8.58 pF between Cor1 and Cor2 pins in Fig. 7. In this case, the unity gain frequency is 1.2 MHz and the phase margin is 53.9°. The graphic chart of Fig. 9 characterizes the noise parameters of the op-amp.

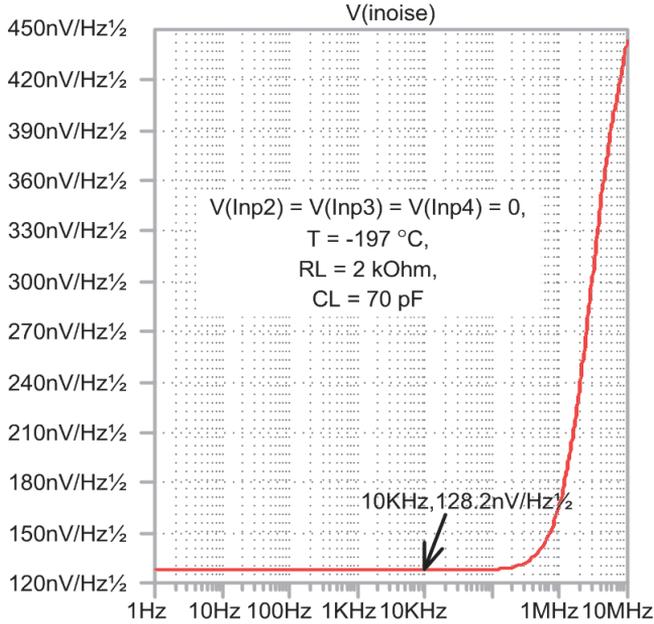


Fig. 9 – Dependence of the Fourier density of the noise voltage of amplifier OAmpl3 on the frequency.

Table 1
The Simulation Results of the DDOA at the Power Supply ± 5 V.

Parameter name	Amplifier name	
	OAmpl3	OAmpl4
Consumption current, mA	0.434	0.434
Input current	<1 fA ¹⁾	<1 fA ¹⁾
Offset voltage, μV	193 (95 ²⁾)	53 (26 ²⁾)
Voltage gain	57640 (115830 ⁴⁾)	210800 (422030 ⁴⁾)
Full output voltage, V	-3.28/3.09	-3.28/3.09
Unity gain frequency, MHz	1.2	2.61
Phase margin at the unity gain, degrees	53.9	6.4
Fourier density of the noise voltage nV/Hz ^{0.5}	128.2	26.0
Note: ¹⁾ evaluation, the typical value of the measured input current of the input p-JFET at 27°C is about 40 pA; ²⁾ at the parallel connection of two input stages		

Table 1 shows the simulation results of DDOA OAmP3, OAmP4 at $T = -197^{\circ}\text{C}$.

DDOA OAmP4 has been developed on the based DDOA OAmP3 (Fig. 7), characterized in that on this circuit in the sources of transistors the input DSs resistors R9, R11, R12, R13 are removed. At the same time, the amplification gain is increased, the noise level is decreased, but the permissible input voltage range is significantly reduced due to the reduction of the linear operation range of the input DSs to 1 V, compared to 3 V for OAmP3.

5 Instrumentation Amplifiers on the DDOAs

Fig. 10 shows the connection of the DDOA OAmP3 in the form of an instrumentation amplifier (IA) [20, 21] indicating the nodes to which the input (Inp1, Inp2), control (Inp4) and NFC (Inp3) signals.

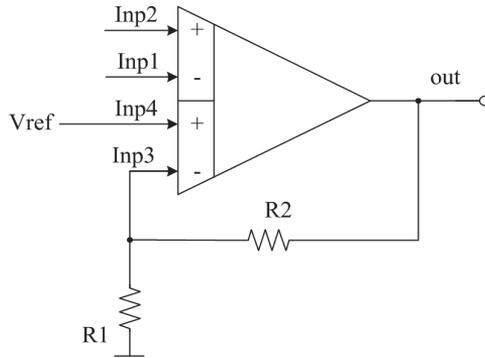


Fig. 10 – Circuit of connection the DDOA OAmP3 as an instrumentation amplifier.

The amplification gain K_V of the AC voltage in the low-frequency region of the IA is determined by the ratio of resistors R2, R1, i.e. $K_V = 1 + R_2/R_1$, and the reference voltage V_{REF} at input Inp4 sets the level of the constant output voltage $V(\text{out}) = (1 + R_2/R_1)V_{REF}$ when there is no input signal.

According to the connection circuit (Fig. 10) simulation of the output signals of IA (Fig. 11) at $R_1 = 1 \text{ k}\Omega$, $R_2 = 4 \Omega$, which explains the possibility of providing at $T = -197^{\circ}\text{C}$ with the required gain and setting the output level of the IA when the reference signal is supplied to the input Inp4.

Thus, the change in the reference voltage at the input of Inp4 from 0 (output signal 2, Fig. 11) to 0.1 V (output signal 3, Fig. 11) leads to a change in the constant level of the output signal of IA from 0 to 0.5 V in accordance with the previously given dependence $V(\text{out}) = f(V_{REF})$.

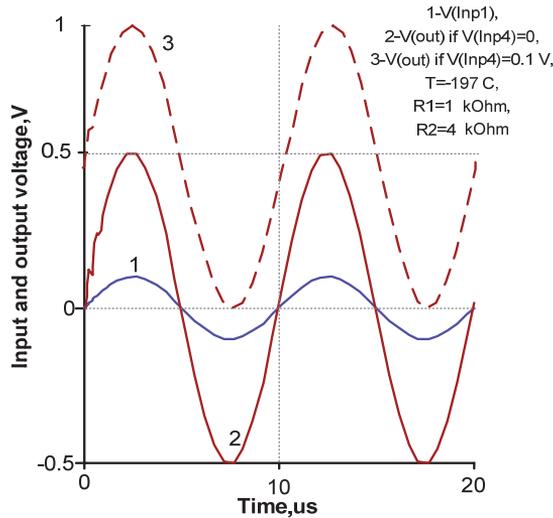


Fig. 11 – Input and output voltage of the IA on the DDOA at a temperature of -197°C and various V_{REF} .

6 Conclusion

Recommendations have been formulated on the design of low-temperature analog ICs based on the elements of the new BiJFet array chip MH2XA030, which are used in the development of two types of differential difference operational amplifiers – OAmP3, OAmP4.

Cryogenic OAmP3 (OAmP4) with the supply voltage of $\pm 5\text{ V}$ and the temperature of -197°C are characterized by the following parameters: the consumption current is less than $500\ \mu\text{A}$, the input current is less than $1\ \text{fA}$, the voltage gain is more than 50.000 (200.000), the offset voltage is less than 200 (60) μV .

On the basis of OAmP3 it is possible to produce instrumentation amplifiers which are the most necessary for cryogenic equipment with the amplification gain of more than 100 , the current-voltage converters with the conversion factor of more than $1\ \text{mV/nA}$, working on the load with the resistance of more than $2\ \text{k}\Omega$ and the capacitance up to $100\ \text{pF}$.

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